

Lab no.20

FOUR-QUADRANT FULL-BRIDGE CHOPPERS

PWM controlled with bipolar voltage switching

1. Introduction

In Lab no.19 was mentioned the possibility of the four-quadrant choppers to cover all quadrants of the electrical plane: output voltage – output current ($U_o - I_o$). If we refer to the output power $P_o = U_o \cdot I_o$ it will result the possibility of the DC/DC converter to exchange electrical energy in both directions, by reversing the output current direction or by reversing the output voltage polarity. So, the converter is both *bidirectional* and *reversible*. The use of the four-quadrant converter in an application is required by the electrical load that must also operate in all four quadrants. For a specific case of an electrical drive with a DC motor the application requires to rotate the motor in both directions with the possibility of braking from any direction and the motion energy recovery. We say that the motor is included in an *adjustable and reversible electrical drive system*.

Also in the previous laboratory papers it was mentioned that the treatises analyses the four-quadrant DC/DC converters (choppers) gradually, starting from the simple *half-bridge structure* (bridge leg) and then proceeds to the more complex *full-bridge structure* (H bridge). In real applications, the four-quadrant half-bridge topology is rarely used due to the disadvantages already known: the need for a double DC source and the possibility of an imbalance between the two voltages during the heavy dynamic modes. These disadvantages can be avoided by using the full bridge structure. Even though this structure is more complex and the number of power semiconductor devices doubles, the advantages obtained compared to the half bridge structure justify the additional investment.

2. Full-bridge structure

The full-bridge structure with controllable power switches is not used in power electronics only to obtain four-quadrant DC/DC converters. This topology is also used to achieve PWM single-phase: inverters, rectifiers and power active filters. As shown in Fig.20.1, the full-bridge topology consists of two bridge legs A and B, each leg being composed of two power transistors (BJT, MOSFET, IGBT etc.) connected in series, provided with recovery diodes connected in antiparallel.

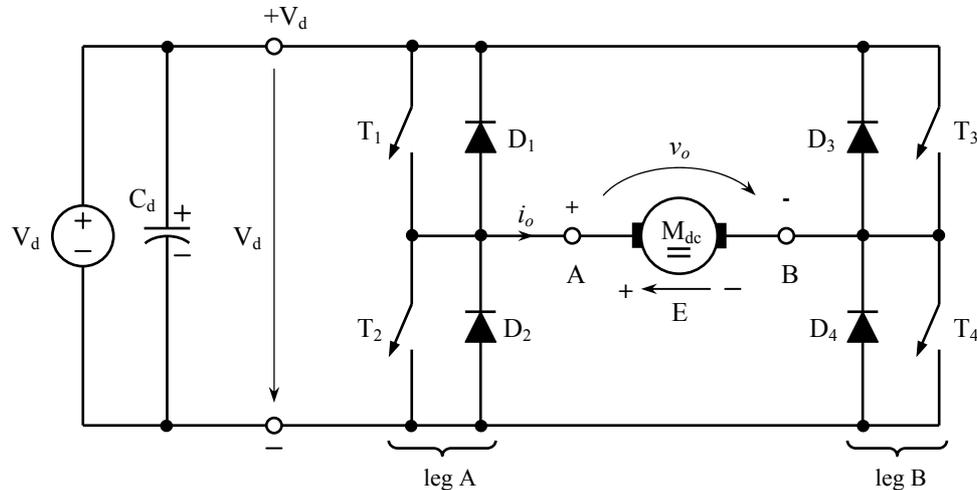


Fig.20.1 Full-bridge topology of a four-quadrant chopper.

Transistors from leg A have been labeled with T_1, T_2 and the ones from leg B with T_3, T_4 . The antiparallel recovery diodes of the transistors were labeled with the same index, D_1, D_2 for leg A and D_3, D_4 for leg B. The full-bridge supply is done with a well-filtered single DC voltage V_d . As close as possible to the full-bridge, the C_d capacity is placed, which, in addition to the role of the voltage filter, has the important role to recover the energy from the load inductance field after each transistor turn-off. Since the transistors have very short switching times, fast capacitors with low equivalent series resistance (low ESR) must be used. The mid-points of the two arms are denoted by A and B. These ones are the output terminals of the structure between which the converter load of $R-L-E$ type (DC motor in the figure $\rightarrow M_{dc}$) is connected. The converter output voltage is noted with v_o , and the output current with i_o .

The control of the transistors from each leg is made using a pair of *complementary* PWM signals. Depending on how the two legs are controlled, we can use two *PWM switching techniques (strategies)* for a full-bridge structure:

- *PWM with bipolar voltage switching*
- *PWM with unipolar voltage switching.*

The two techniques listed above can be used for the full-bridge choppers and also for the single-phase PWM inverters or rectifiers. Each of these converters will operate differently, depending on the PWM switching technique used. Also, the conversion quality is changed from a technique to another. For this reason the converters analysis will be done separately for each control strategy. Next, the full-bridge chopper will be analyzed using the first control strategy.

3. PWM control technique with bipolar voltage switching

For the PWM control technique with bipolar voltage switching, the transistors on the H bridge diagonal are grouped in pairs: T_1 with T_4 , T_2 with T_3 . So, when the pair (T_1, T_4) is turned on the pair (T_2, T_3) is in off-state and vice versa. Consequently, for the four power transistors only two PWM control signals are needed: PWM_1 for pair (T_1, T_4) and PWM_2 for pair (T_2, T_3) . In practice, complementary PWM signals with dead time (blanking time) are used. It is a simple and easy way to implement this control strategy, reason for what it is widely used in applications, even it is less performance.

For this control strategy, during a switching period T_s , four operation sub-cycles of the full-bridge structure can be highlighted. They are given by the four output currents paths i_o in a T_s cycle of operation. In Fig.20.2, these paths are marked with numbers from 1 to 4.

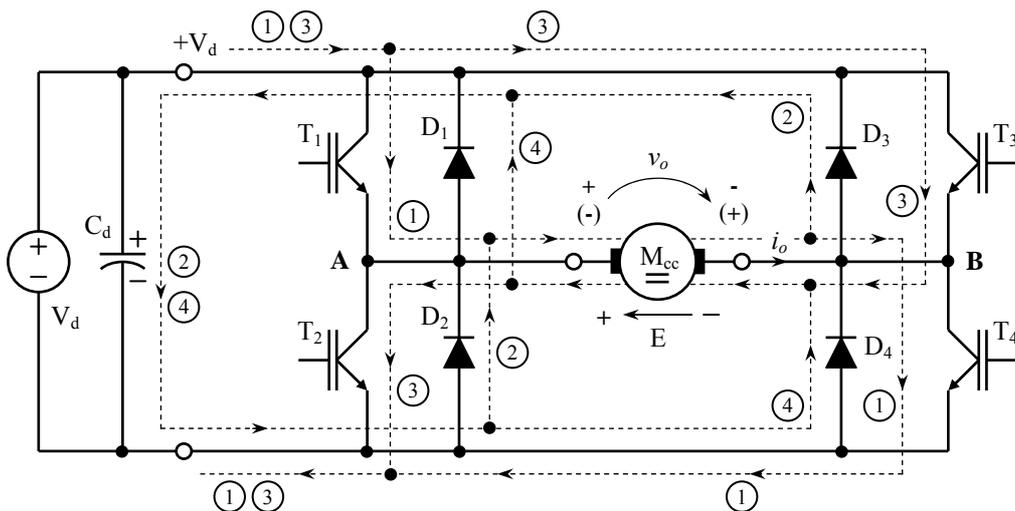


Fig.20.2 Current paths for a full-bridge chopper PWM controlled with bipolar voltage switching.

Waveforms corresponding to the output voltage v_o and the output current i_o of the full-bridge chopper are identical to those for half-bridge four-quadrants chopper shown in the Lab no.19 - Fig.19.2. In order not to repeat that figure, in Fig.20.3 the waveforms will be presented for the real case, when the voltage drop across the devices in conduction is taken into account. The v_o voltage waveform deviations from its ideal form presented in Fig.19.2 becomes more evident as the V_d voltage is low (volts or tens volts order). Since on all the four current paths two semiconductor devices are in conduction, transistors or diodes, voltage drops of $(2\div 6)V$ order occur that may affect visible the waveform of the voltage v_o as shown in Fig.20.3.

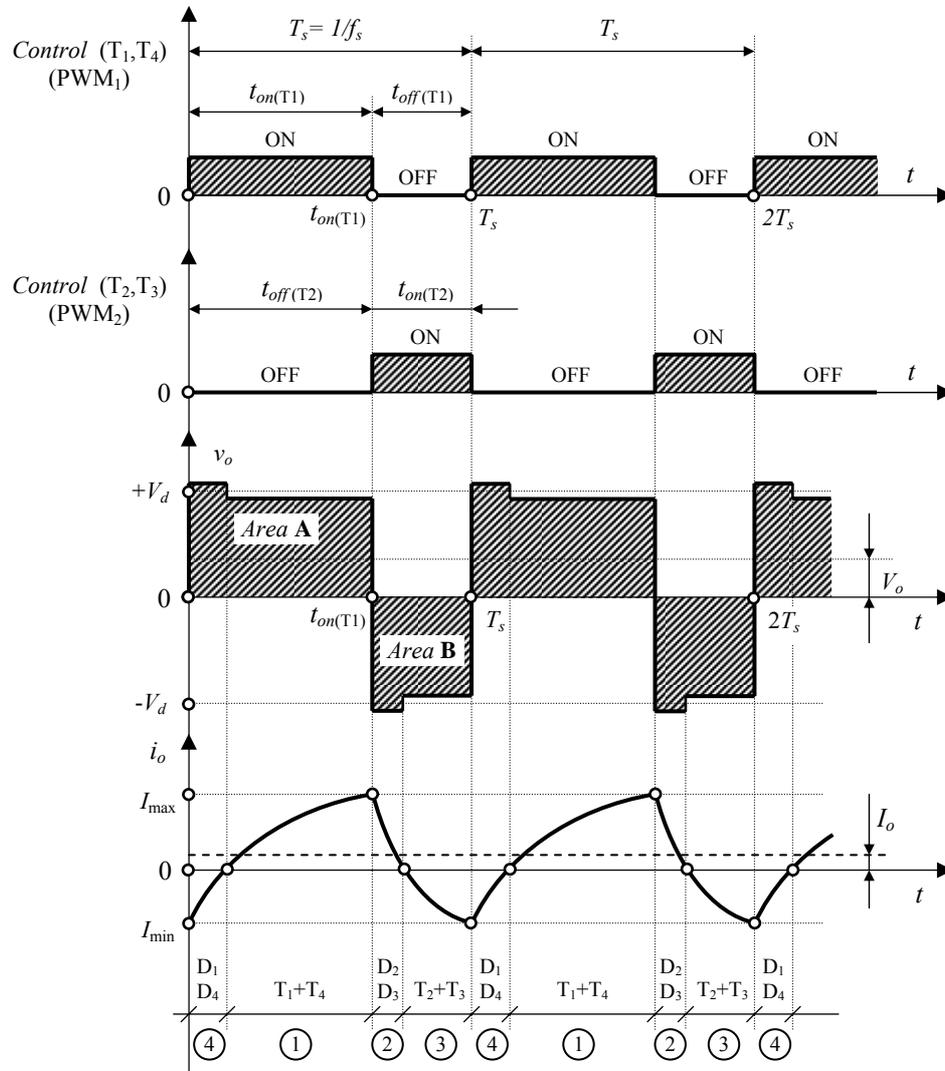


Fig. 20.3 Real waveforms corresponding to the full-bridge *chopper* PWM controlled with bipolar voltage switching.

In the (1) operating subcycle the (T_1, T_4) transistors are in conduction. The current i_o flows on the route labeled with (1) in Fig.20.2. The V_d voltage is applied to the DC motor (with the „+” potential on the left terminal and the „-” potential on the right terminal), but with a slightly lower value due to the voltage drops on the two conduction transistors:

$$u_o(t) = V_d - 2 \cdot V_{on(T)} \rightarrow \text{during the time interval (1) in Fig.20.3} \quad (20.1)$$

The i_o current will evolve in time following an increasing exponential, as shown in Fig.20.3. Calculation of the $i_o(t)$ expression is presented in the Lab no.19, equation (19.9). For an exact calculation we can use for the output voltage the real value given by the (20.1) equation. As shown in Fig.20.3, the i_o current is positive during the (1) time interval which creates an electromagnetic torque, also positive in the DC motor ($T_{em}>0$). The same i_o current will cause power losses in the motor resistance R_a and an energy accumulated in the L_a inductance field.

As soon as the pair of transistors (T_1, T_4) is turned off, the i_o current cannot flow further on path (1) and it will seek a recovery path, noted with (2) in Fig.20.2. The (D_2, D_3) diodes are turned on when the inductance L_a generates a self-induced voltage with reverse polarity (polarity in brackets of the v_o voltage) based on the energy stored in its field. This voltage must balance the V_d **voltage and the voltage drops across the two diodes**. Thus, in subcycle (2) of Fig.20.3 the real value of the output voltage is:

$$u_o(t) = -V_d - 2 \cdot V_{on(D)} \rightarrow \text{during the time interval (2) in Fig.20.3} \quad (20.2)$$

In the subcycle (2) a part of the energy stored in the L_a inductance field is consumed by the motor being converted into motion (kinetic) energy by keeping a positive electromagnetic torque ($i_e > 0$) during this time interval, another part is transferred to the capacity C_d and the last part is converted into heat by the resistance R_a . As the inductance energy decreases the current drops gradually, following a decreasing exponential curve. Its expression is given by equation (19.11) from the Lab no.19, where the value V_d is replaced by $V_d + 2U_{on(D)}$.

When the energy from the L_a inductance field is depleted the current i_o becomes zero at the end of the time interval (2). After this moment the pair (T_2, T_3) becomes, at last, to conduct the i_o current on the path (3) in Fig.20.2. Thus, the converter output current becomes negative determined by the E electromotive voltage and by the V_d supply voltage reverse connected to the motor terminals. The voltage v_o remains negative but with a lower amplitude than $-V_d$ due to the voltage drops across the two on transistors:

$$v_o(t) = -V_d + 2 \cdot V_{on(T)} \rightarrow \text{during the time interval (3) in Fig.20.3} \quad (20.3)$$

In subcycle (3) the i_o current will continue to follow the decreasing exponential from subcycle (2), but with a less slope due to the smaller v_o negative voltage after passing from the subcycle (2) into subcycle (3). The i_o current evolution towards a steady state value of the decreasing exponential is interrupted when (T_2, T_3) transistors are turned off. At the end of subcycle (3) the inductance L_a has accumulated in its electromagnetic field an energy corresponding to the current value $I_{min} < 0$. This energy will maintain the i_o current flow through the recovery diodes (D_1, D_4) on the path noted with (4) in Fig.20.2. Thus, the output voltage jumps from the negative value given by (20.3) to the positive value:

$$v_o(t) = V_d + 2 \cdot V_{on(D)} \rightarrow \text{during the time interval (4) in Fig.20.3} \quad (20.4)$$

As in the case of subcycle (2), in subcycle (4) the energy from the inductance field is transferred to the motor shaft and to the C_d capacity, reason for that the negative amplitude of the output current is decreasing until it reaches zero value, when whole of the energy was consumed. After this time the pair of transistors (T_1, T_4) begins to conduct a positive current determined by the supply voltage V_d . Thus, the full-bridge operates again in subcycle (1).

The time evolution of the output current in subcycle (4) follows an increasing exponential which will also continue in subcycle (1) of the next switching time period. The expression $i_o(t)$ is given by the equation (19.9) from the Lab no.19 where V_d is replaced with $V_d - 2V_{on(T)}$ for a converter analysis under realistic conditions.

It is noticed that during its operation, at $t_{on(T1)}$ and T_s time moments, the output voltage of the full-bridge structure suddenly changes its polarity, fact that led to the name of PWM control strategy *with bipolar voltage switching*.

It is difficult to calculate the average value of the real v_o voltage waveform shown in Fig.20.3, because the time intervals (1)-(4) are variable, depending on the i_o current evolution required by the load (random variable). Thus, if the supply voltage V_d is not of volts order, it can be approximated that during subcycles (1) and (4) $v_o(t) = +V_d$ and during subcycles (2) and (3) $v_o(t) = -V_d$. In addition, it will be considered that the power transistors switch instantly and the control signals are complementary without a dead time, as shown in Fig.20.3. Based on the latest assumptions, the relation between the duty ratios of the two transistor pairs is:

$$t_{on(T1)} + t_{on(T2)} = T_s \Leftrightarrow \frac{t_{on(T1)}}{T_s} + \frac{t_{on(T2)}}{T_s} = 1 \Rightarrow d_{(T1)} + d_{(T2)} = 1 \quad (20.5)$$

In the above simplified terms the average voltage (DC voltage) from the output of a full-bridge chopper is obtained with the help of the same equation as in the case of the four-quadrant half bridge chopper:

$$\begin{aligned} V_o^{not} = \text{average value of } v_o(t) &= \frac{1}{T_s} \int_0^{T_c} v_o(t) \cdot dt \approx \frac{1}{T_s} \int_0^{t_{on(T1)}} (+V_d) \cdot dt + \frac{1}{T_s} \int_{t_{on(T1)}}^{T_c} (-V_d) \cdot dt = \\ &= \frac{\text{Area A} + \text{Area B}}{T_s} = \frac{1}{T_s} \cdot \left[V_d \cdot [t]_0^{t_{on(T1)}} - V_d \cdot [t]_{t_{on(T1)}}^{T_s} \right] = V_d (2 \cdot d_{(T1)} - 1) \end{aligned} \quad (20.6)$$

where: $d_{(T1)} = t_{on(T1)} / T_s$ is **duty ratio** of the transistors pair (T_1, T_4).

Since $0 \leq t_{on(T_1)} \leq T_s$ then $0 \leq d_{(T_1)} \leq 1$. Taking into account the equation (20.6) we obtain:

$$0 \leq d_{(T_1)} \leq 1 \Rightarrow -V_d \leq V_e \leq +V_d \quad (20.7)$$

The equation (20.7) shows the **reversibility** property of the full-bridge chopper PWM controlled with bipolar voltage switching. Consequently, the DC motor supplied by such a DC/DC converter can be turned in both directions with variable adjusted speeds.

It can be seen that the output current waveform of a full-bridge chopper is similar to the output current waveform of a two-quadrant chopper or of a half-bridge four-quadrant chopper. Therefore, the average value (DC current) I_o can be calculated with the same approximately equation presented in previous labs:

$$I_o \approx (I_{max} + I_{min})/2 \quad (20.8)$$

Depending on how the extremes I_{max} and I_{min} are placed the *average output current can be positive or negative*, so the full-bridge chopper is **bidirectional**. Taking into account the reversibility property mentioned above, it means that the DC machine can be accelerated, rotated and braked in both rotating directions, which is equivalent to its operation in the four quadrants of the mechanical torque-speed plane ($n - T_{em}$). In Fig.20.4 we can see all four quadrants of the electrical and mechanical plane, where the converter-motor system can operates.

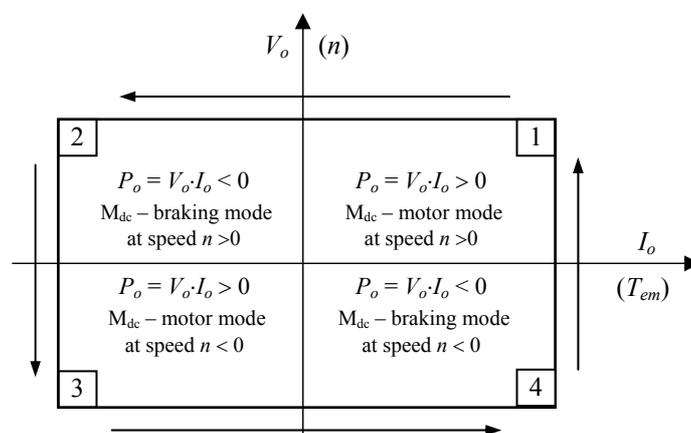


Fig.20.4 The 1÷4 quadrants of the electrical and mechanical plane in which the converter-motor system can operates.

How the converter-motor system passes in anticlockwise direction through the four quadrants is described in Lab no.19. The electromagnetic and electromechanical transient modes of the system are identical even if the four-quadrant DC/DC converter is changed.

4. Laboratory application

In the Power Electronics Laboratory there are available several full-bridge structures made with power transistors (MOSFET, IGBT). They were designed with all the necessary facilities for the laboratory experiments (flexibility, easy access to the measurement points, control and feed-back signals compatible with modern μC or DSP digital control systems, electrical isolation between the power and the control blocks, multiple protection functions, start/stop circuits, etc.). One of these full-bridges is designed as a distinct module which does not include the driver circuits and is used in laboratory setup to study the four-quadrant full-bridge chopper controlled PWM with bipolar voltage switching. The block diagram of the laboratory stand is shown in Fig.20.5 and the image during its operation is shown in Fig.20.6.

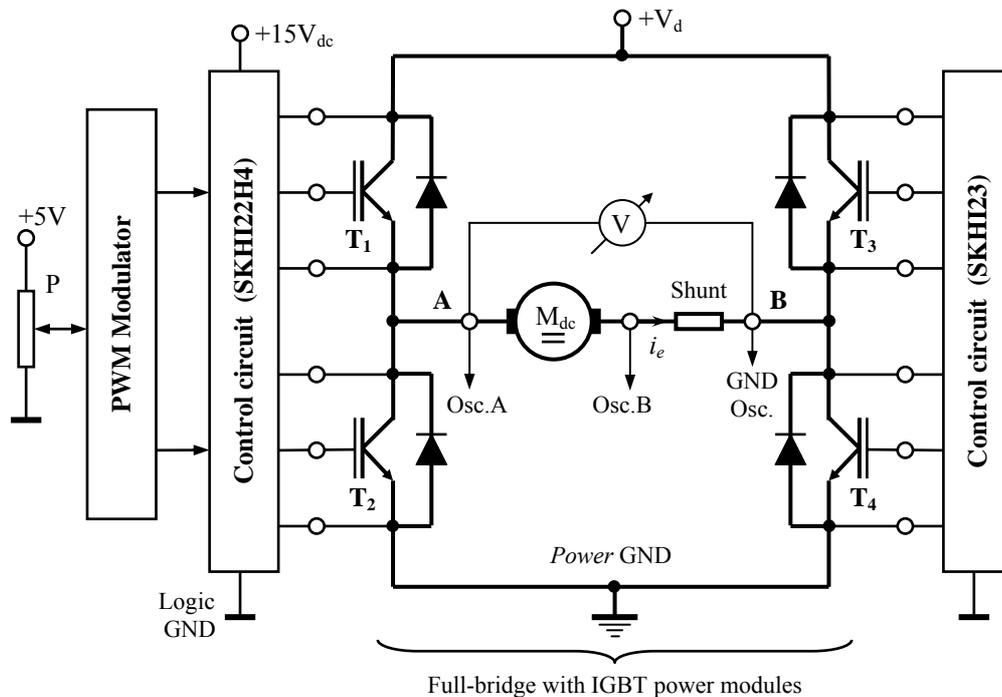


Fig. 20.5 Block diagram of the laboratory setup for full-bridge chopper study.

The full-bridge structure is achieved with IGBTs. They are used as integrated modules (PIM), with half-bridge structure, SKM50GB123D type, manufactured by *Semikron*. The catalogue data of the transistors are: collector current 50A and 1200V maximum collector-emitter voltage. Each of two half bridge IGBT power modules was mounted on a heat sink. Further, both bridge legs are mounted on a plate in a position that suggests the H bridge structure, as shown in the image of Fig. 20.7(a). On

the same plate are mounted: the dv/dt R-C snubbers for each transistor, the connectors for the control terminals, respectively for the power terminals (connectors for $\pm V_d$ bus and for A and B outputs).

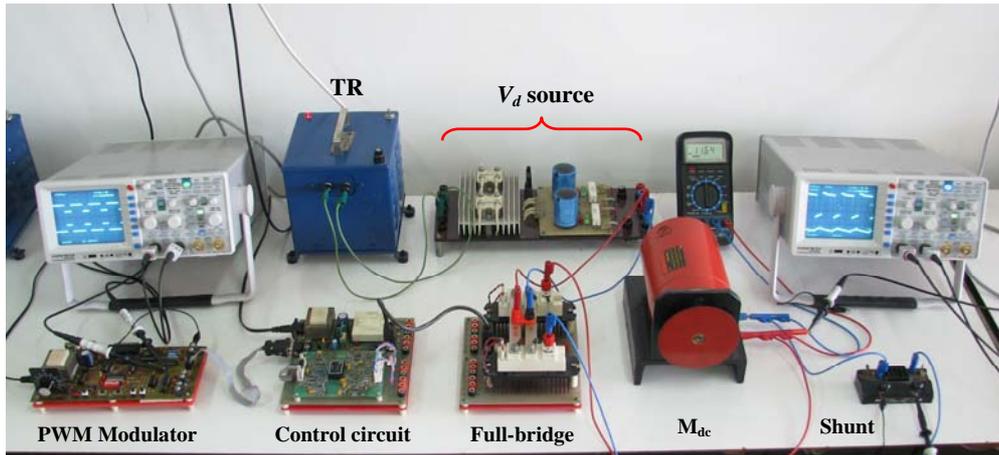


Fig.20.6 Image of the laboratory application.

To control the IGBT transistors included in the full-bridge structure it will be used the control circuit studied at Lab no.6 whose image is reproduced in Fig.20.7(b). The control circuit includes the MOS gate driver modules SKHI22H4 and SKHI23, both manufactured by *Semikron*. As mentioned before, these drivers are identical in terms of operation (different mode of integration) and each of them can simultaneously control two power transistors included in a bridge leg (half-bridge structure). Thus, with the help of the whole control circuit, described in Lab no.6, we can control the two bridge legs included in the full-bridge structure.

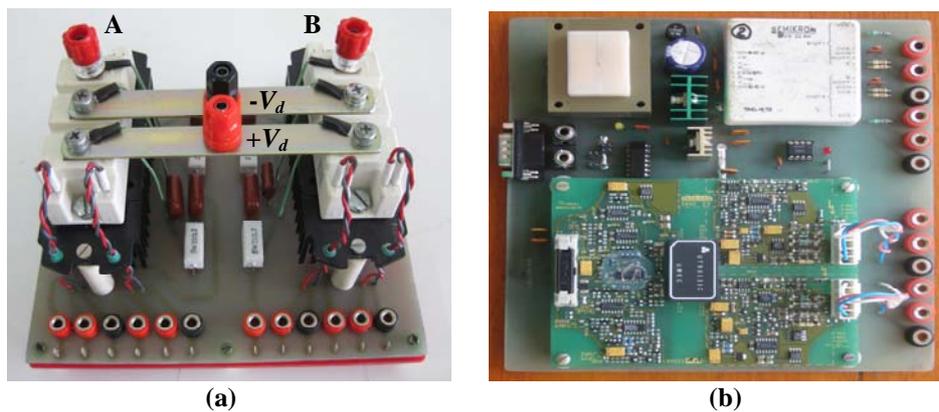


Fig. 20.7 (a) Image of the full-bridge structure achieved with IGBT power modules.
 (b) Image of the control circuit achieved with SKHI - MOS gate drivers.

The experimental setup also contains the voltage source $U_d (= 30V_{dc})$ which is described in Lab no.16. It should be noted that besides the grid transformer (TR), the single-phase diode rectifier and the capacitive filter, the source includes a *braking resistance* having the role to consume the energy recovered during the braking mode of the DC motor. The PWM control with bipolar voltage switching of the full-bridge structure is obtained with the help of two PWM logical signals, PWM_1 and PWM_2 , generated by the PWM modulator described in Lab no.17. The connection between the control circuit and PWM modulator is made with a ribbon cable with two standard couplings at both ends. To achieve the laboratory setup we also used: two oscilloscopes with two channels, a voltmeter to measure the average output voltage of the chopper, a shunt to display the current waveforms, wire provided with banana connectors, etc. With the help of the first oscilloscope we can display simultaneously the two complementary PWM signals with dead time (PWM_1 and PWM_2), and with the help of the second oscilloscope we can display the output voltage and current (u_o , i_o). In Fig.20.6 we can see this signals pair which are identical with the theoretical waveforms presented in Fig.20.3.

5. Objectives and procedures

1. It will be studied the theoretical aspects related to full-bridge chopper controlled PWM with bipolar voltage switching (topology, operating, waveforms, voltage and current equations);
 2. It will be performed the experimental setup for the full-bridge chopper with the topology shown in Fig.20.5 and the image shown in Fig.20.6;
 3. It will be displayed with the help of the first oscilloscope the waveforms of the two complementary PWM signals with dead time generated by the PWM modulator – there are measurement points on the board of the modulator;
 4. It will be displayed with the help of the second oscilloscope the waveforms of the output voltage v_o and of the output current i_o which should result as the diagrams shown in Fig.20.3;
 5. The bipolar switching of the output voltage v_o and deviation from the ideal waveform will be observed;
 6. The duty ratios of the pairs (T_1, T_4) and (T_2, T_3) will be slowly modified and it will be observed:
 - V_o average value variation measured with the help of a voltmeter and the DC motors speed with the change of the duty cycle of the two complementary PWM signals;
 - changing of the V_o polarity if the duty ratios of the two transistor pairs is changed around the value of 0.5;
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7. It will be modified suddenly the duty ratios of the two transistor pairs, (T_1, T_4) , respectively (T_2, T_3) and it will be observed
 - the increasing of I_o during the motor acceleration when the duty ratio of the transistors pairs is suddenly modified in opposite directions from the value of 0.5;
 - the decreasing of I_o and its reversal flow direction (transient braking) when the duty ratios of the transistor pairs of is suddenly moved closer from different directions to the 0.5 value;
8. It will be highlighted the possibility of the DC motor to operate in all four quadrants of the mechanical plane with quick accelerating and braking modes in both directions;
9. It will be examined and compared the experimental i_o currents waveform with the waveform shown in Fig.20.3 to confirm that it is composed by exponential segments, waveform more visible as the switching frequency decreases;
10. It will be manually braked the motor during the rotation and it will be observed the increase of average current value I_o , either to the positive or to negative values, depending on the rotation direction;
11. It will be set a low switching frequency (about 1 kHz) of the PWM modulator and it will be observed the change of the output current ripple with the duty ratio changing of the PWM signals. It should be noted that the maximum ripple is obtained for a duty ratio of 0.5 for both transistor pairs;
12. It will be increased the switching frequency and it will be observed how the ripple current is reduced - the current filtering effect increases with the switching frequency.

References:

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