

Lab no. 3

**THYRISTORS AND TRIACS CONTROL
GATE TRIGGER CIRCUITS**

1. Introduction

The thyristor is a power semiconductor device with the control terminal called grid or gate (G). The device name comes from the similarity of operation with the gas triode: *thyratron transistor*. Because the thyristors are mainly used in the controlled rectifier structures, the technical literature calls them as SCR (*Semiconductor Controlled Rectifiers*) devices.

After the series manufacture start in 1957 until the '80s of the twentieth century the thyristor was the leader of power semiconductor devices with control electrode. Despite the fact that the thyristor is a half controlled device (through the gate terminal can be only turned on) this switch remains favourite in a wide range of applications because it is robust, can be easily controlled and can operate in high power structures at high voltages and currents with low power conduction losses.

To operate, every thyristor require a drive (trigger, control) circuit that provides gate current pulses to induce the on-state. These pulses must have a certain amplitude and duration. The device remains latched in on-state until it is reverse biased. Thus, in forward biased conditions, after the turn-on process, the gate current can be interrupted.

Thyristors can be found in various applications such as phase-controlled rectifiers, AC voltage variators, starters, static breakers, cycloconverters, etc. Depending on the requirements, are available on the market several types of thyristors: common thyristors (used in phase-controlled converters at low switching frequency, high voltages and currents), fast thyristors (with a small blocking time), optical thyristors (light-activated through optical fibers), etc.

A triac can be equivalent with two antiparallel connected thyristors. Thus, the control principles and the control circuits of the triacs are the same as those of the thyristors taking into consideration that the triacs are bidirectional devices (the current can flow in both directions through them).

2. The symbol and the semiconductor structure of the thyristors

The thyristor symbol is similar with the diode symbol at which, besides the power terminals anode (A) and cathode (K), a grid terminal (G) is added - Fig.3.1 (a). The current through the thyristor Th , denoted by i_{Th} in figure, flows only in one

direction from the anode to the cathode if the power device is forward biased. Voltage drop across the thyristor, the anode-cathode voltage, may be noted by v_{Th} or v_{AK} .

The semiconductor structure of a thyristors, shown in Fig.3.1(b), contains four alternating layers: $p-n-p-n$. To obtain this “silicon wafer”, first are generated by diffusion the two p layers at the ends of a flat silicon cylinder, lightly doped with pentavalent atoms (n^- type). By metallization of the anode surface with aluminium atoms, the heavy doped p^+ layer is obtained in order to reduce the contact resistance between semiconductor chip and the anode metal disc shown in figure. The cathode applied to the other end of the silicon cylinder is made as a metal ring that surrounds the electrode grid. The cathode ring is applied over a circular area of n^+ type obtained by alloying the gate layer with the electron donor metals.

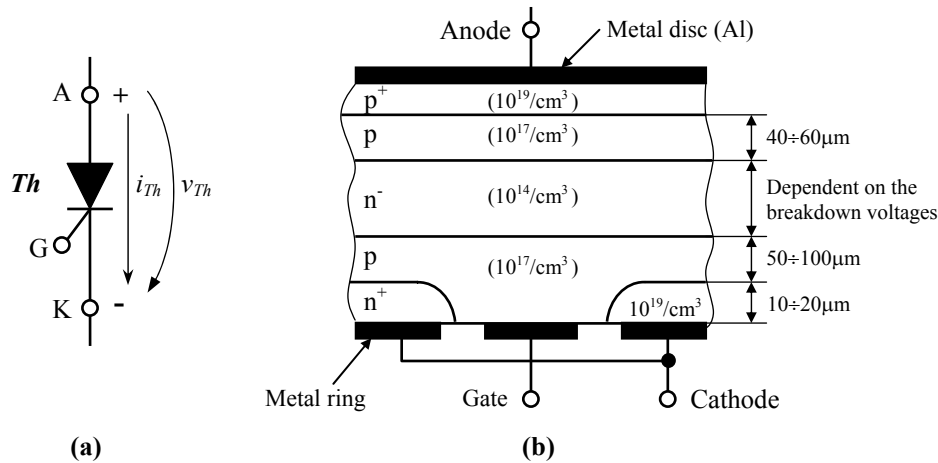


Fig. 3.1 The symbol (a) and the semiconductor structure (b) of a thyristor.

The ratio between the diameter and height of the semiconductor cylinder (chip) is very high. The thickness of the layers, especially of the n^- layer that has the roll of a drift region, depends on the operating voltages for which the thyristor was made. No matter how great are these voltages, the overall height of the chip shown in Fig.3.1 (b) is of the order of millimetres. Unlike the height, the diameter of the silicon cylinder depends on the maximum current that can flows through the thyristor. In the case of thyristors made for thousands of amperes the diameter can reach values of the order (8÷10) cm. These devices have a special shape for the grid (stellar shape) to increase the turn-on speed.

The silicon chip is closed in a capsule whose roll is to give mechanical resistance and protection for the device, to sustain the terminals and to assure the heat transfer between the chip and the radiator. The capsule part that can be mounted on the radiator can be connected to any of two power terminals. Thus, can be

manufactured thyristors, either with the cathode, either with the anode connected to the radiator. This option helps a lot in the manufacture process of the thyristors bridge structures.

3. The equivalent circuit and volt-ampere static characteristics

To understand the operating mode of a thyristor is very useful to find an equivalent circuit that can approximate the behaviour of this device, both in static and dynamic states. Fig.3.2 shows the imaginative operations made on the thyristor semiconductor structure to obtain the equivalent circuit. In Fig.3.2(a) is presented a simplified structure of a thyristor with the four semiconductor layers $p_1-n_1-p_2-n_2$ separated by three junctions J_1, J_2 and J_3 . If the median layers n_1 and p_2 are imaginary splitted, as shown in Fig.3.2(b), without lost the electrical connection, two distinct structure are obtained, the first $p_1-n_1-p_2$ corresponds to a pnp bipolar junction transistor (BJT) and the second $n_1-p_2-n_2$ corresponds to a npn type BJT. By replacing these structures with the BJT symbols results the equivalent circuit of a thyristor, shown in Fig.3.2(c). Based on this scheme one can deduce the static characteristics of the power device and it can be explaining the turn-on process initiated through the gate terminal (by the gate pulse current).

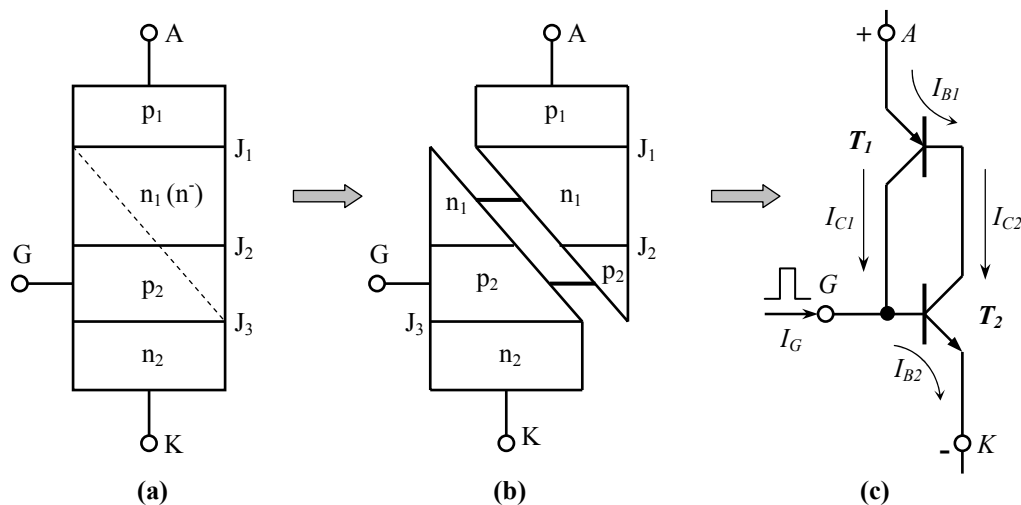


Fig. 3.2 The equivalent circuit deduction starting from the thyristor semiconductor structure.

When a negative voltage is applied on the thyristor ($u_{Th} < 0$) the equivalent transistors T_1 and T_2 are reverse biased and the current through these devices can be considered zero. In fact, there appears a very low leakage current of the microampere order. If the reverse voltage exceeds the V_{BR} (**R**everse **B**reakdown **V**oltage) value, an

important reverse current appear. This current increase steeply to a value only limited by the external circuit – see Fig.3.3. To avoid such situations in a certain application, the thyristors are chosen according to the **Maximum Repetitive Reverse Voltage** V_{RRM} (catalogue parameter), less than the breakdown voltage ($V_{RRM} < V_{BR}$).

In the case of a forward bias ($u_{Th} > 0$) and in the absence of the control signal the thyristor remain in off-state because the two equivalent transistors can not be turned on. Thus, the operating point is placed on the *forward blocking characteristic* where the power device can sustain forward voltages under the **Breakover Voltage** (V_{BO}) value – see Fig.3.3(a). Usually, from the manufacturing process, it results a breakdown voltage approximately equal with the reverse breakdown voltage ($U_{BR} \approx U_{BO}$).

The thyristor conduction mode may be induced if one of two equivalent transistors is turned on. The base currents I_{B1} and I_{B2} of the transistors T_1 and T_2 can flow if the complementary transistor is in on-state. It is sufficient to apply a short current pulse between the gate and cathode terminals ($i_G > 0$) to bring the transistor T_2 in on-state that initiates an **avalanche turn-on process** of the entire power device. Thus, after the transistor T_2 is turned on the collector current I_{C2} appear, which is, in fact, the base current of the T_1 transistor ($I_{B1} = I_{C2}$). Consequently, the transistor T_1 is also turned on and its collector current I_{C1} increases even more the base current of the T_2 transistor. The growth of the I_{B2} current will lead to the increase of the collector current I_{C2} and so on. There is a positive reaction illustrated in Fig.3.3(a) by the translations of the operating point from the forward blocking characteristic to the forward conduction characteristic.

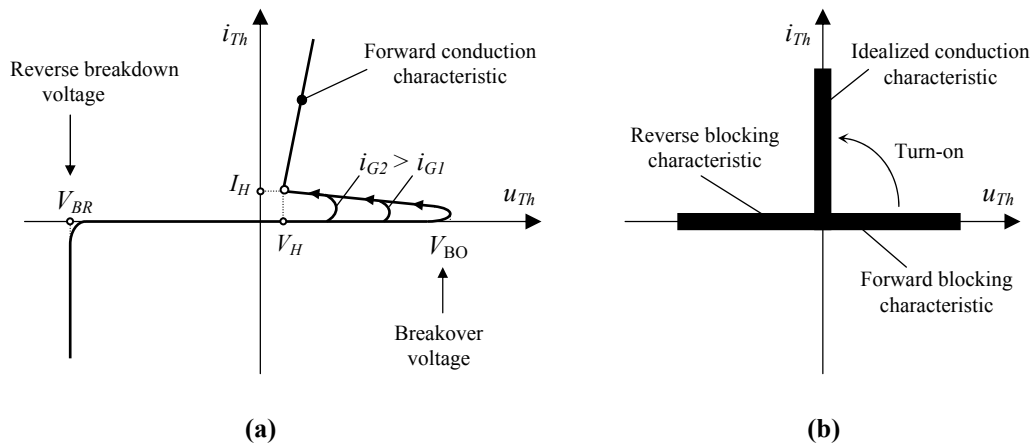


Fig. 3.3 (a) Real i - v characteristics; (b) Idealized i - v characteristics of the thyristors.

Then the thyristor current (anode current) reach a threshold value: $i_{Th} = I_H$ (*holding current* – catalogue parameter) the gate current (i_G) can be removed.

Therefore, the control signal of the thyristors appears as a short pulse current. To accelerate the turn-on process this pulse can have, in the first moment, a greater amplitude. Then the amplitude must decrease to a value supported by the gate-cathode junction in a continuous mode.

In forward blocking state and in reverse blocking state the leakage current through thyristor can be approximate to be zero. Thus, it is obtained the two characteristics specified of a ideal switch: the forward and the reverse blocking characteristics, shown in Fig.3.3(b). Also, the forward conduction characteristic can be approximate with an idealized characteristic because the on-voltage is reduced to a thyristor, in range of (1÷3)V. The higher values belong to the high power thyristors.

4. Thyristors and triacs control technique

Fig.3.4 shows the simplest structure of a controlled rectifier, the half-wave rectifier. The topology includes a thyristor T_h whose power terminals, anode (A) and cathode (K), are connected in a loop which includes, besides the semiconductor device, an AC source (v_s) and a load. For simplicity we will chose a purely resistive load consisting only of the R resistance.

To understand the converter operation, the thyristor can be regarded as a unidirectional switch that comes into conduction (on-state) when a short current pulse is applied between the grid (G) and cathode terminals by a specialized block called **gate control circuit** or **gate trigger circuit** (GTC). Once in on-state, the thyristor maintains its status as long as is kept the forward bias (“+” on the anode and ”-“ on the cathode). The blocking state (off-state) of the thyristor (interruption of the current flow) **can not be induced** through the control terminal by the GTC.

Analyzing the polarities of the v_s source from Fig.3.4(a) it is evident that the turn-on can be achieved only in the time intervals when the thyristor is forward biased, more precisely, during the positive half-waves (polarity outside of the parentheses).

If the thyristor is replaced with a power diode, his turn-on occurs **naturally** at the beginning of each time interval when this device become forward biased. For this reason the left limits of the positive half-waves (points P in Fig.3.4 (b)) can be called **natural commutation points**.

Definition: *The natural commutation points locate the moments after that the devices from a power structure supplied with an AC voltage are forward biased and can be turned on.*

The thyristors can be turned on even in the natural commutation point moments (where the converter behaviour is identical with the same diode converter) or can be turned on with a certain delay from the natural commutation points.

Definition: The **control (phase, delay) angle**, usually denoted by “ α ”, is a delay from the natural commutation point, expressed in electrical degrees, after that the thyristors or the triacs are turned on.

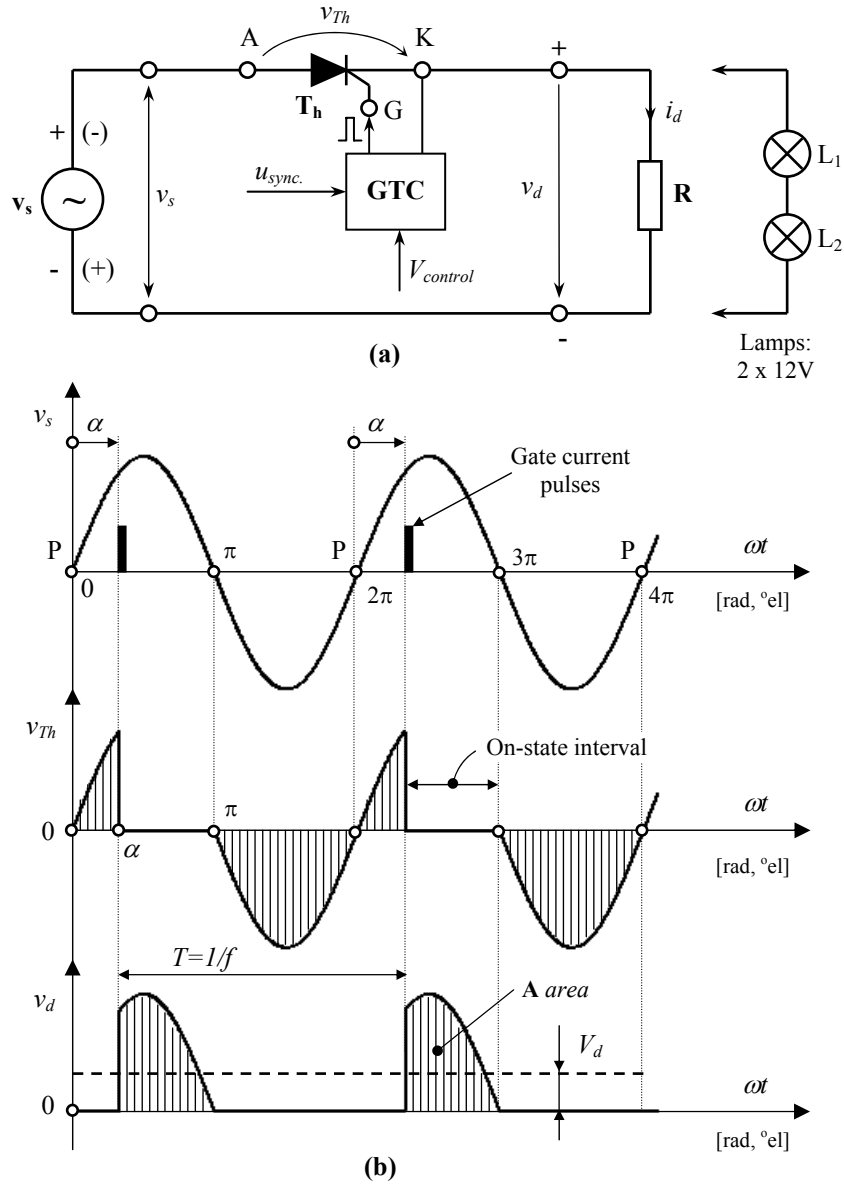


Fig. 3.4 Thyristors phase-control principle (technique).

To control the converter with a certain α angle, the gate trigger circuit must be able to know (locate) the moments in time defined as natural commutation points. For this reason the gate control circuit includes, among other functions, the **synchronization function**. This function is implemented using the u_{sync} signal synchronized with v_s supply voltage obtained with the help of a **sync transformer**. The α value is imposed by a **control (shift) voltage** ($V_{control}$) applied at the input of the gate trigger circuit.

Definition: *This synchronized (in phase) control with a regulated phase angle obtained with the help of the gate trigger circuits can be defined as phase-control technique of the thyristors or of the triacs.*

5. Controlled rectifying principle

Fig.3.4(b) shows the waveforms of the half-wave rectifier presented in Fig.3.4(a) when it is controlled with a certain angle $\alpha < 180^\circ$ and when it supplies a purely resistive load. This load can be implemented in the laboratory using a rheostat (R) or a group of incandescent lamps (L_1 - L_2). The lamps are preferred because after the delay angle modification the effect is visible, spectacular, the light intensity is changed.

On the time intervals in which the T_h thyristor is in off-state its impedance can be considered infinite and the i_d current is, practically, zero. Consequently, the voltage drop across the resistive load (converter output voltage v_d) is zero. The entire supply voltage is taken by the thyristor. After the thyristor is turned on, using the gate current pulses, we find almost the entire supply voltage at the converter output, across the resistive load. For the analysis simplicity, we consider the thyristor as an ideal device that can switch instantly and it has a zero voltage drop in on-state.

Since the converter load is purely resistive, the i_d current waveform is the same with the v_d voltage waveform. When the supply voltage v_s crosses zero to the negative half-wave the current through the thyristor (i_d) is stopped. After this moment there are met **the conditions for the thyristor turn-off: reverse biased of the device for a longer period than the blocking time (t_q - catalog parameter) and zero value for the thyristor current.**

Once that the thyristor is turned off, it takes all the negative half-wave and a portion of the positive half-wave until the gate current pulse appear in the next period T of the AC voltage. In this way, across the load resistance, we only find portions of the positive half-waves (output voltage pulses), shorter or wider, depending on the angle control value (see Fig.3.4.(b)):

$$v_d(t) = \begin{cases} 0 & \text{pentru } 0 \leq \omega t < \alpha \\ \sqrt{2} \cdot V_s \sin \omega t & \text{pentru } \alpha \leq \omega t \leq \pi \\ 0 & \text{pentru } \pi < \omega t \leq 2\pi \end{cases} \quad (3.1)$$

where : V_s is the rms value and $\omega=2\pi f$ is the pulsation of the AC supply voltage.

These output voltage pulses are repeated with a T_p period, equal with the AC voltage period: $T_p=T=1/f$. Because the pulses **have not** an alternative waveform around the ωt axis, it is obvious that the periodically output voltage v_d contain a DC component, noted with $V_{d\alpha}$, whose value can be calculated with the average value formula applied to a periodic signal:

$$V_{d\alpha}^{\text{not}} = \text{average value of } v_d(t) = \frac{1}{T_p} \int_0^{T_p} v_d(t) \cdot dt = \frac{1}{T} \int_0^T v_d(t) \cdot dt \quad (3.2)$$

If in the (3.2) equation is performed the following variable change $\omega t = x$ the integral limits result: $\left\{ \begin{array}{l} \text{for } t_1 = 0 \Rightarrow x_1 = \omega \cdot t_1 = 0, \\ \text{for } t_2 = T \Rightarrow x_2 = \omega \cdot t_2 = (2\pi/T) \cdot T = 2\pi \end{array} \right.$

Thus, the (3.2) equation becomes:

$$\begin{aligned} V_{d\alpha} &= \frac{1}{2\pi} \int_0^{2\pi} v_d(t) \cdot dt = \frac{1}{2\pi} \left(\int_0^{\alpha} 0 \cdot dt + \int_{\alpha}^{\pi} \sqrt{2}V_s \sin x \cdot dt + \int_{\pi}^{2\pi} 0 \cdot dt \right) = \\ &= \frac{1}{2\pi} \left(\int_{\alpha}^{\pi} \sqrt{2}V_s \sin x \cdot dt \right) = \frac{1}{2\pi} \cdot \text{Area } \mathbf{A} = \frac{\sqrt{2}U_s}{2\pi} \cdot (-\cos x) \Big|_{\alpha}^{\pi} = \\ &= \frac{\sqrt{2} \cdot V_s}{2\pi} \cdot (\mathbf{1} - \cos \alpha) \geq \mathbf{0} \quad \text{for } 0 \leq \alpha \leq \pi \end{aligned} \quad (3.3)$$

The result of the (3.3) equation highlights the following observations:

- Getting a nonzero average values for the output voltage ($V_{d\alpha} \neq 0$) suggests that the simple electronic circuit shown in Fig.3.3(a) makes an AC/DC conversion, so it is an electric-electric static converter, a half wave rectifier. For this reason the variables from the DC side: voltage, current, power, etc. are written with the "d" index.
- The output average DC voltage $V_{d\alpha}$ **can be adjusted through the phase angle α** (phase-controlled rectifier);

6. Control circuits for thyristors and triacs

As a controlled turn-on device, the thyristor cannot operate without a control circuit. Its role is to provide current pulses between the gate and the cathode terminals to start the device turn-on at the desired moments. In case of the complex power structures, with many thyristors, a single control circuit is preferred to ensure trigger

current pulses for all thyristors. This distinct block of the power electronic system is, usually, called **gate drive circuit** or **gate trigger circuit** (GTC).

Since a triac is equivalent with two antiparallel connected thyristors, the control principles for the thyristors and the circuits that implement these principles can be used, also, for the triacs.

The GTCs can be achieved with the help of low power discrete components or using specialized integrated circuits (eg. UAA145). The trigger control circuits manufacturing without dedicated integrated circuits can be justified today only for simple applications, such as the structures with a single low power thyristor or triac. Choosing a trigger control circuit with discrete components in this case becomes more economical. For example, the single-phase AC voltage variators often use the control trigger circuits made with the unijunction transistors.

In the complex power electronic equipments the control unit must implement multiple functions. Consequently, to decrease the size and the price of the power electronic systems and to increase the operating performance, modern integrated drivers are used to control the thyristor or other power semiconductor devices. As described in the previous section, for the thyristors, these integrated gate drivers must be able to achieve the phase control of the thyristors, preferable during the both half-waves of the AC voltages. The most used integrated circuit that implements these requirements is UAA145 phase control circuit, whose block diagram is shown in Fig.3.5. It should be noted that these integrated can not operate alone, without any circuit components around them. First, an UAA145 integrate require for supply a stabilized source with two DC voltages ($\pm 15V_{dc}$) and a montage scheme that include discrete components: resistors, capacitors, diodes, low-power transistors etc. With the help of these external components the user can impose some of the operating parameters (e.g. trigger pulse duration).

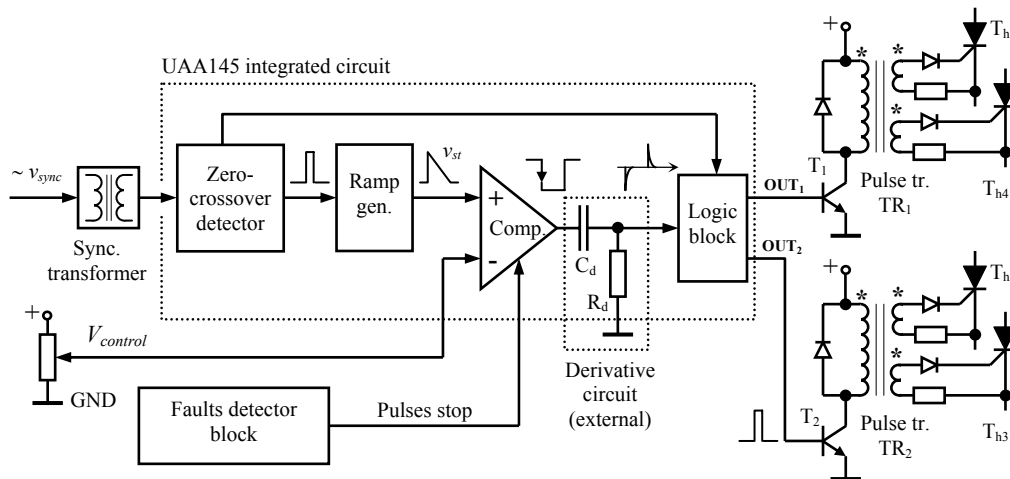


Fig. 3.5 The control circuit block diagram for a single-phase rectifier (full bridge structure with the $T_{h1} \div T_{h4}$ thyristors).

Usually the gate trigger circuits (GTCs) for thyristors perform the following operating functions:

- synchronization function
- voltage – time conversion function
- pulse generating function
- electrical isolation function
- protection function

To implement these functions the GTC can be structured in a functional block diagram as shown in Fig.3.5. This gate driver is able to control a power structure with thyristors or triacs supplied by a single AC voltage. It was considered the case of a single-phase full-bridge rectifier with four thyristors $T_{h1} \div T_{h4}$. For a three-phase full-bridge rectifier the control circuit must contain three of such schemes.

a) **Synchronization function** is performed by the first block that is the zero-crossover detector. As the name suggests, it detect the crossings of the synchronization (sync) voltage through zero. At the output of the zero-crossover detector, zero-voltage switching pulses (sync pulses) are obtained which locate in time the natural commutation points, P for the positive half-wave and N for negative half-wave (see Fig.3.6). The sync voltage is in phase with the AC voltage that supplies the power structure. Usually, it is obtained from that with the help of a sync transformer that provides electrical isolation and also, adapts the sync voltage amplitude to the requirements of the GTC.

b) **Voltage – time conversion function** allows to adjust the α phase angle by means the control voltage $\rightarrow V_{control}$. The conversion technique of an electrical quantity (a voltage value) in a time interval (electrical angle) is based on the comparison of a voltage ramp with a control voltage (see Fig.3.6). The voltage ramp (increasing or decreasing) is generated during the time intervals when the thyristors are forward biased (during the time interval when the control circuit can send trigger pulses delayed with the α angle from the natural commutation points). Because the UAA145 integrated circuit provides decreased voltage ramps during every half-cycle of the AC voltage, at the output of the ramp generator block is obtained the, so-called, sawtooth signal (v_{st}). Thus, the GTC can control multiple thyristors with the same α angle, both the thyristors forward biased during the positive and the negative half waves of the supply AC voltage. The v_{st} signal is obtained across a capacity that is discharged slowly in time. If a linear ramp is desired the discharge process must be done with a constant current obtained with the help of a constant current generator made with a low-power external transistor (see Fig.3.9).

$$\left. \begin{array}{l} v_{st} = \frac{1}{C} \cdot \int i_c \cdot dt \\ i_c = I_c = const. \end{array} \right\} \Rightarrow v_{st} = \frac{1}{C} \cdot \int I_c \cdot dt = \frac{I_c}{C} \cdot \int dt = K \cdot t \quad (K = const.) \quad (3.1)$$

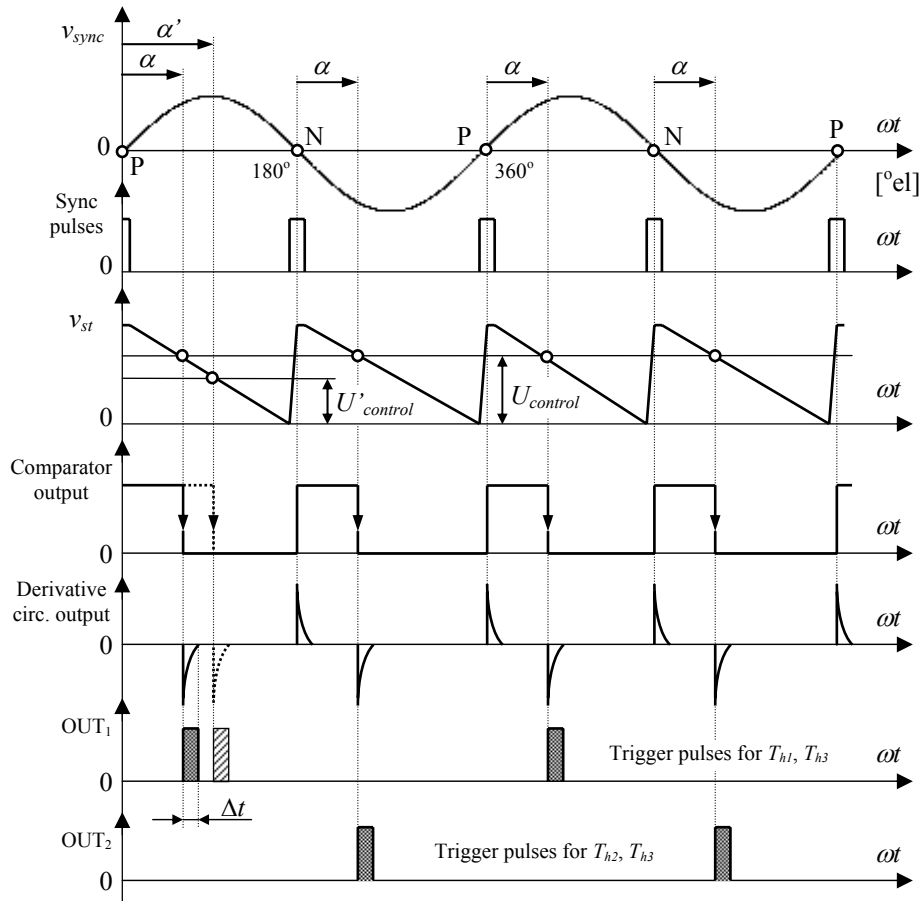


Fig. 3.6 Waveforms corresponding to the gate trigger circuit presented in Fig.3.5.

The equation (3.1) shows that, by discharging the capacitance C at constant current ($i_C = I_C = const.$), a linear evolution of the voltage across the capacity is forced ($v_{st} = K \cdot t$ - a line equation). *The linearity of the sawtooth signal ramp ensures the linearity of the transfer function of the gate trigger circuit: $\alpha = f(V_{control})$.*

For a sawtooth signal with decreasing ramp version, as shown in Fig.3.6, during the zero-crossover (sync) pulses the C capacity is suddenly charged. Since the charging process can not be achieved instantaneously, the sync pulses must persist for a minimum time interval to allow the capacity voltage to reach the desired amplitude of the sawtooth signal. If the zero-crossover pulse duration is greater than a minimum optimal value, a time interval appear in which the sawtooth signal is cut (the maximum amplitude of the tooth is maintained). During this time interval it can not send trigger pulses on the thyristor gate. For this reason, the width of the zero-crossover pulses must be carefully adjusted via some exterior components of the

integrated trigger circuit. In conclusion, from Fig.3.6 results that the width of the zero-crossover pulses limits the regulated interval of the phase angle, both minimum and maximum:

$$0 < \alpha_{\min} \leq \alpha \leq \alpha_{\max} < 180^{\circ} \quad (3.2)$$

If the control precision requirements are small it can be use a simpler and cheaper version that replaces the constant current generator with a discharge resistance. In this case, the sawtooth ramp is nonlinear (R-C circuit) which determines the nonlinearity of the trigger circuit transfer function. To reduce this nonlinearity, a discharge to a negative voltage is used. Thus, the ramp is the first part of an exponential curve which can be considered quasi linear.

For the variant of a sawtooth signal with an increasing voltage ramp at the end of each half-cycle, the capacity must be suddenly discharged. Thus, during the zero-crossover pulses the capacity is prepared for a new increased voltage ramp. Also, in this case, the sync pulses width limits the adjusting range of the α phase angle.

The sawtooth signal v_{st} is applied at the noninverter input of a comparator (Comp.) and at the inverter input is applied the control voltage $V_{control}$. When the instantaneous voltage ramp equals the $V_{control}$ voltage the comparator switches and a decreasing step appear in the waveform of its output logical signal. This decreasing front of the signal locates in time the moment when the trigger pulse must be applied on the thyristor gate. Fig.3.6 shows how the delay (phase) angle is adjusted from α to α' value if the control (shift) voltage changes from $V_{control}$ to $V'_{control}$. It is a suggestive illustration of the voltage-time conversion.

c) Pulse generating function allows to generate trigger pulses with a certain Δt width and amplitude after the decreasing front appears in the waveform of the comparator output signal. This function, which in logical circuits' domain can be achieved by a monostable circuit, is obtained by the UAA145 with the help of a external RC derivative circuit. Thus, the fronts of the comparator output signal are converted into derivate pulses whose shape is shown in Fig.3.6. Their duration, which imposes the width of the trigger pulses, can be adjusted by the time constant of the derivative circuit ($\tau = R \cdot C$). Only the helpful pulses (negative) obtained at the output of the derivative circuit are used by the next stage. This stage, the logic block circuit, is designed to alternatively distribute the trigger pulses to the outputs OUT₁ and OUT₂, depending on the half wave which occur. In this way, the thyristors receive the trigger pulses when they are directly biased.

d) Electric isolation function between the GTC and the power structure of the power electronic systems is very important because it ensures both the personnel safety during the maintenance operations when the circuit is in function and the circuit protection against the perturbations induced by the power structure. In low power and voltage applications, the electric isolation function can be neglected.

To fulfill the GTC electrical isolation function the output pulses are sent to the thyristor gate through a pulse transformer. These circuit elements, with relative low power, (10÷20)VA, presents the following advantages over the optocoupler version:

- it does not require an additional energy source;
- by using a transformer with multiple secondary windings the same trigger pulses can control more thyristors simultaneously.

In Fig.3.5 the final stage of a GTC for a single-phase full-bridge thyristors rectifier is shown. Its topology consists of four thyristors, denoted with Th_1 , Th_2 , Th_3 and Th_4 (see Lab no.8). The Th_1 , Th_4 thyristors are triggered during the positive half-wave, while Th_2 , Th_3 thyristors are triggered during the negative half-wave. For each thyristors pair, a single pulse transformer was used, each having two secondary windings for the both thyristors.

The primary winding of the pulse transformers are supplied with the help of low-power transistors denoted with T_1 and T_2 in Fig.3.5 which, in turn, are driven by the outputs of the integrated circuit, OUT_1 and OUT_2 , respectively. The pulse transformers must be well dimensioned, so that, the widest trigger pulse do not cause the transformers saturation, an equivalent situation to a short circuit through the transistors. Each primary windings of the pulse transformer must be accompanied by an antiparallel diode that discharges the energy from the transformer electromagnetic field, after the transistors turn-off. During the discharge time interval the current through the primary winding decreases and the derivative of the magnetic flux changes its sign ($d\Phi/dt < 0$). Therefore, the negative voltage pulses appear in the secondary winding. To protect the gate-cathode junction (J_3) against reversed uncontrollable voltages, a diode is used in each secondary circuit, as shown in Fig.3.5. The resistance from this circuit limits the gate current during the used positive pulses.

e) Protection function is implemented using a faults detection block. This block must be able to monitor some variables from the power structure, such as: the currents which flow through the thyristors, the converter output current, the supply voltages, etc. A simplest such block should include the short-circuit protection. When a fault is detected, the trigger pulses must be stopped. Usually, the comparator included in the integrated circuit is blocked.

It should be noted that, for power structures with thyristors, the protection acts with some delay because the devices in conduction at a moment, when the fault occurs, must withstand over-currents until the turn-off conditions are met: the reverse bias. Practically, the protection function is useful only for thyristors which should be turned on further. For this reason, the protection systems for the power structures schemes must be completed with other protection types, such as, ultra fast fuses.

7. The montage scheme for the UAA 145 gate trigger integrated circuit

The specialized UAA145 gate trigger circuit dedicated to the thyristors and triacs control is designed as a monolithic integrated circuit enclosed in a capsule (DIP16 – special case) whose shape and the pins configuration are shown in Fig.3.7. Its functional block diagram, presented in Fig.3.8, is similar to the simplified block diagram from Fig.3.5 upon which has been introduced and described the functions of a gate trigger circuit for thyristors and triacs.

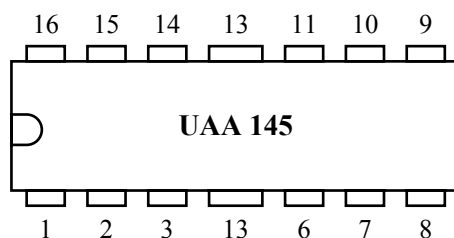


Fig. 3.7 Capsule of the UAA145 integrated circuit.

The pins significance of the UAA145 integrated circuit is:

1 – Positive voltage supply (+Vcc)	10 – Output pulse - negative half-wave
2 – Comparator output	11 – Derivative circuit output
3 – Ground (GND)	13 – Negative current supply (I)
6 – Pulse inhibit	14 – Output pulse - positive half-wave
7 – Sawtooth (ramp) signal (v_{st})	15 – Reference negative voltage (-8V)
8 – Control (shift) voltage (for α angle)	16 – Sync (zero-crossover) pulses
9 – Synchronization input	

The internal connections of the above mentioned pins with the functional blocks of the UAA145 are shown in Fig.3.8. The figure also presents the external circuit elements (resistances, potentiometres capacities etc.) which accompany the integrated circuit for its proper functioning. All these elements are integrated in a montage (operating) scheme for the integrated circuit. Through them the user can adjust the operating parameters of the UAA145 in a specific application. Further, it will be listed of the circuit elements from the montage scheme and for each one it will be briefly presented its functional role:

- **The voltage divider R_1 - R_2** , connected to pin 9, through which the sync pulses duration is adjusted. Depending on the divider resistances (the ratio of division), a certain fraction of the v_{sync} is applied at the crossover detector input. This block generates sync (zero crossover) pulses only during the time intervals when the u_{sync} fraction passes through zero and it is within the range

(-0.7)÷(+0.7)V. Obviously, by changing the amplitude of the u_{sync} fraction with the help of the R_1 - R_2 divider it was changed the time interval in which the voltage applied to pin 9 is located in this voltage range and thus it can be adjusted the sync pulses width. During the sync pulses the external C_2 capacity is charged to the required peak of the sawtooth signal (+8V). If the sync pulses are too narrow the C_2 capacity fails to charge up to 8V amplitude and if the sync pulses are too wide the sawtooth signal appears cut. Consequently, the range of the α delay angle shrinks.

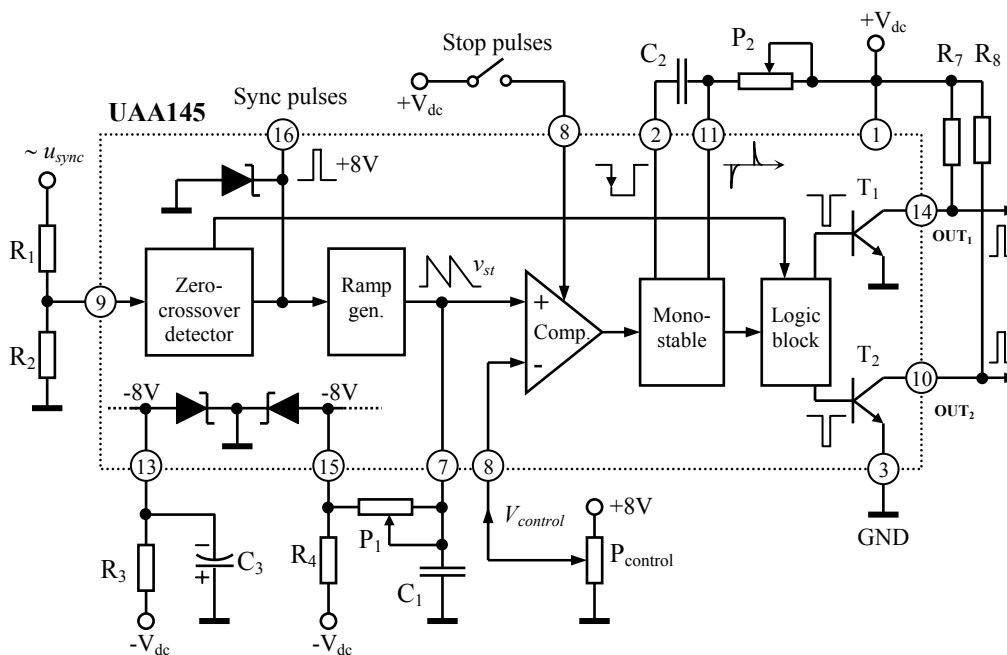


Fig. 3.8 Block diagram and the montage scheme of the UAA145 gate trigger integrated circuit.

- **R_3 – C_3 group** allows to obtain a negative stabilized voltage (-8V) from the negative supply voltage ($-15V_{dc}$) applied to pin 13 through the R_3 resistance. The stabilization is achieved using a Zener diode synthesized into the internal structure of the integrated circuit. C_3 capacity is used as a power buffer and voltage filter
- **P_1 – C_1 group** allows to generate the v_{st} sawtooth signal. At each zero crossing of the sync voltage, the C_1 capacity is quickly charged at an 8V voltage and after this it is discharged slowly through the P_1 potentiometer to obtain the decreasing ramp of the sawtooth signal. In order to get a quasi linear ramp it was used a trick that consists in the C_1 discharging toward a -8V potential obtained at the pin 13 in the same way as to the pin 15. From the exponential curve it is used only the first part, until 0V potential. In this way it can be

generated a ramp almost linear (see the voltage-time conversion function). If a strictly linear ramp is demanded in special applications, instead the P_1 potentiometer it can be used a constant current generator. By means of P_1 the discharge current can be modified and so, the slope of the ramp of the sawtooth signal can be adjusted.

- $P_2 - C_2$ group together with the internal monostable block set the width of the output trigger pulses. At the pin 2 it is obtained a square signal and at the pin 11 it is obtained this signal derived by the $P_2 - C_2$ (see Fig.3.6). Useful are only the negative pulses which appear due to the decreasing fronts of the square signal. These negative pulses are taken by the logic block, are formed and distributed alternately to the 14 and 10 outputs in correspondence with the half-waves of the sync voltage. By means of P_2 potentiometer it can be adjusted the trigger pulses width.
- R_7 and R_8 resistances without whom the trigger pulses can not be obtained because the UAA145 integrated circuit has the open collector type outputs. This is a feature that gives flexibility in applications, because it can be used different types of final stages which follow the integrated circuit (see lab diagram).

Apart from the circuit elements listed above, the montage scheme of the UAA145 may also include a control potentiometer ($P_{control}$) that provides the shift voltage applied to the pin 8 and a switch with the help can be stopped the trigger pulses. These elements may be replaced by a digital control microsystem, respectively by a scheme that implements protection functions, as described in section 6.

8. Laboratory application

In order to study the UAA145 operation, to display the pins waveforms and to draw the transfer function $\alpha = f(V_{control})$, in the Power Electronics Laboratory are available more gate drivers achieved with this integrated circuit. The schematic circuit of such gate trigger, conceived as a laboratory board, is presented in Fig.3.9 and the image is shown in Fig.3.10. This has three stages: the source, the montage scheme of the UAA145 integrated circuit and the final stage.

a) DC source

It is a stabilized DC source with two fixed output voltages ($\pm 15V_{dc}$). The source contains a grid transformer with two secondary windings which supply a bridge rectifier and provides, in the same time, the sync voltage. The midpoint of the secondary windings sets the zero potential (ground – GND) of the source. With this source structure, shown in Fig.3, on the C_1 and C_2 capacities, two unregulated DC voltages are obtained. In order to stabilize these voltages, the monolithic voltage regulators were used: LM7815 for the $+15V_{dc}$ and LM7915 for the $-15V_{dc}$.

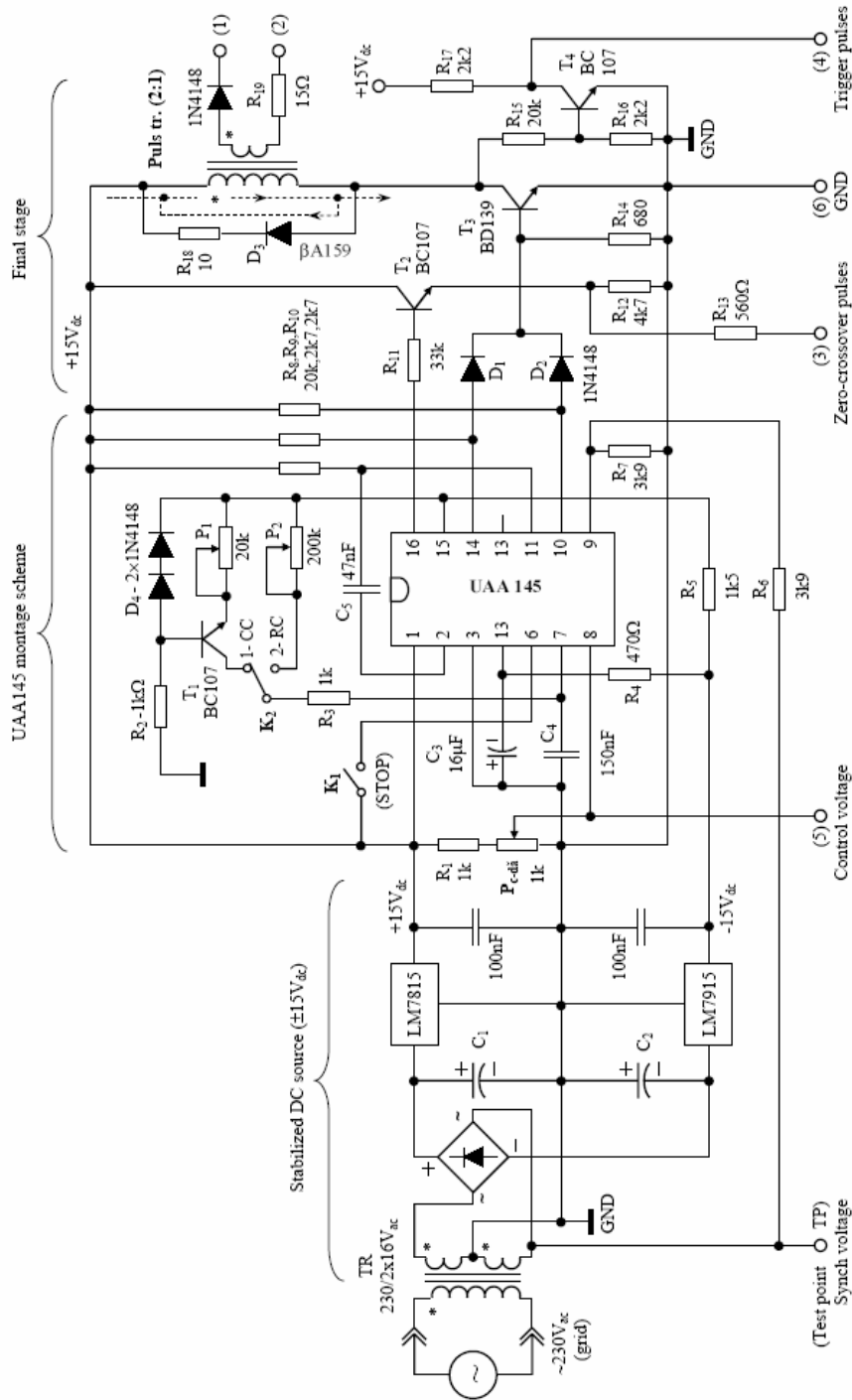


Fig. 3.9 Laboratory board schematic dedicated to study the UAA145 phase control integrated circuit.

b) Montage scheme of the UAA 145

In the middle part of the laboratory board diagram we recognize the montage scheme (circuit) of the UAA 145 with all circuit elements described in section 7. For the sawtooth signal generation it was used a switch (K_2) that can select the discharge of the C_4 capacity toward the pin 15 through a constant current generator (CC - position 1) or through a resistance which consist of the P_2 potentiometer (RC - position 2). As was mentioned in the previous section, a constant current allows a linear discharge of the capacity and therefore a linear ramp for the sawtooth signal. Thus, it was obtained proportionality (linear transfer function) between the control voltage and the α delay angle. In the case of the capacity discharge through the P_2 potentiometer the sawtooth ramp is an exponential fragment determining a nonlinear transfer function between de $V_{control}$ and α .

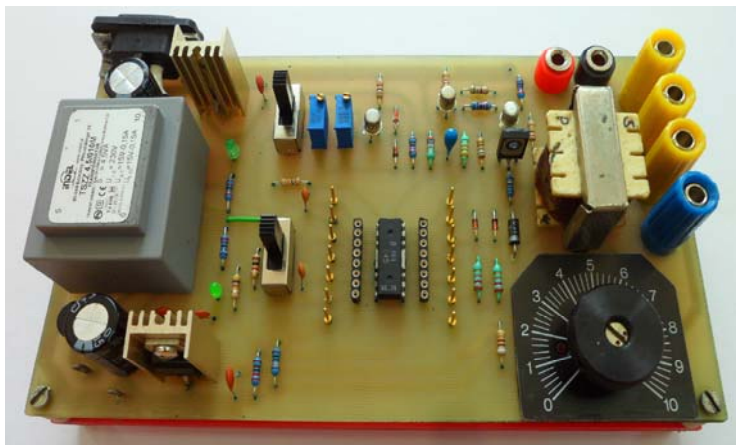


Fig.3.10 Image of the laboratory board dedicated to study the UAA145 gate trigger integrated circuit.

The constant current generator it was achieved with the help of a transistor (T_1), a variable resistance (P_1) and two series diodes (D_4) direct biased by a resistance (R_2). Across the diodes it was obtained a constant voltage that imposes, also, a constant voltage drop on the potentiometer P_1 , so a constant current must flows through it. This is the current that discharge the C_4 capacity.

c) Final stage

The final stage of the laboratory board is designed to capture the useful signals from the UAA145 in order to process and to amplify them for a directly thyristor triggering, for an easy signals display by an oscilloscope or for the delay

angle measure. Thus, the output pulses obtained at the pin 10 and pin 14 are summed by an OR logic circuit (D_1+D_2) and applied on the base of the T_3 transistor to be transmitted at the pulse transformer. During each trigger pulse the T_3 transistor is turned on and the primary winding of the transformer are supplied between the $+15V_{dc}$ and the GND potentials. As long as the transformer does not enter into saturation, the current through the primary winding increases exponentially which leads to the magnetic flux increases and hence to the appearance of the positive trigger pulses in the secondary winding, electrically isolated from the control circuit. After the T_3 transistor is turned off the current through the transformer must flow a certain time interval to discharge the energy from the magnetic field. For this purpose the discharge diode D_3 is used. During the discharge process, the magnetic flux decreases and in the secondary winding a negative voltage pulse occurs. Since on the thyristor gate it must apply only positive trigger pulses, a diode is introduced into the gate circuit. Also, a resistance (R_{19}) is inserted in this circuit to limit the current pulses through the anode-cathode junction.



Fig. 3.11 Gate trigger circuit with UAA145 for different single-phase rectifiers (with maximum 4 thyristors – see Fig.3.5) ; (a) inside case picture; (b) front case picture.

During the trigger pulses the T_3 transistor is on and T_4 is off. Thus, on the collector terminal of the last one we can see synchronous pulses with the output pulses generated by the pin 10 and pin 14. These added pulses can be used by a digital phase meter to measure the delay angle α because they set in time the end of the phase angle. To set in time the beginning of the α delay angle the zero-voltage switching pulses (sync pulses) are used which are obtained at the pin 16 of the integrated circuit. Because the catalog recommends a very low current absorbed from the pin 16, these sync pulses are taken by an emitter repeater ($T_2+R_{11}+R_{12}$) and applied to a banana socket. All the useful signals are brought outside of the board at these types of measured connectors (see Fig.3.9).

The gate trigger circuit whose images are presented in Fig.3.11 uses two pulse transformers, separately controlled by the outputs 10 and 14 of the UAA145, as shown in Fig.3.5. Each pulse transformer, in turn, has two secondary windings, electrical isolated. Thus, we can control up to four thyristors simultaneously (two during positive half-wave

and two during negative half-wave) integrated in different single-phase rectifiers: midpoint rectifier, controlled full-bridge rectifier, half-controlled full-bridge rectifier.

5. Objectives and procedures

1. It will be studied, from the first part of this laboratory essay, the theoretical aspects related to the thyristors: symbol, semiconductor structure, static characteristics, etc.
2. It will be analyzed the thyristors equivalent circuit and the turn-on possibility using the current trigger pulses.
3. It will be analyzed the phase control technique of the thyristors.
4. It will be studied the general aspects of the gate trigger circuits for thyristors and triacs: functional block diagram, specific functions and waveforms.
5. It will be analyzed carefully the block diagram of the UAA145 gate trigger integrated circuit and its montage scheme with the role of each circuit element.
6. It will be analyzed the board schematic circuit dedicated to the laboratory studies of the UAA145 and it will be identified the circuit elements, the test points and the measured connectors.
7. It will be displayed with the help of a two spots oscilloscope the waveforms of each UAA145 pin in correspondence with the sync voltage and these will be compared with the waveforms theoretically presented in this laboratory essay. The sawtooth signal v_{st} will be displayed in two cases corresponding to the two positions of the K_2 switch.
8. It will be highlighted, using a two spots oscilloscope, the adjusting possibility of the shift angle between the sync pulses and the trigger pulses modifying the shift (control) voltage $V_{control}$.
9. It will be drawn the input-output characteristic (transfer function) of the gate trigger circuit: $\alpha = f(V_{control})$ for the two positions of the K_2 switch. The $V_{control}$ voltage it will be measured using a voltmeter connected between measured sockets (5) and (6). The delay angle α will be measured using a digital phase meter connected as follows:

<u>Phase meter</u>		<u>Laboratory board</u>
Channel 1	-----	Banana socket (4)
Channel 2	-----	Banana socket (5)
GND	-----	Banana socket (6)

The data will be introduced in a table with the form:

$V_{control}$ [V]	
α [°el]	



Fig.3.12 Image of the laboratory set-up by means of which it can be displayed the waveforms and it can be drawn the transfer function $\alpha = f(V_{control})$ of the UAA145.

10. It will be performed the experimental circuit shown in Fig.3.4(a) to study the thyristors phase-control technique. As a resistive load it will be used two incandescent lamps (see Fig.3.13);
11. It will be displayed simultaneously the v_s and v_d voltages and it will be measured the average (DC) component of the output voltage (V_{da}) with a voltmeter connected in parallel with the load resistance. It will be highlighted how it is obtained a controlled rectifying by changing the delay angle α and therefore the area of the v_d voltage pulses;
12. It will be highlighted the V_{da} adjustment through the delay angle by means of the voltmeter and the light intensity of the incandescent lamps;
13. It will be drawn the real control characteristic $V_{da} = f(\alpha)$ by measuring the output DC voltage and the delay angle, simultaneously. It will be compared this real characteristic with theoretical characteristic drawn using the equation (3.3).

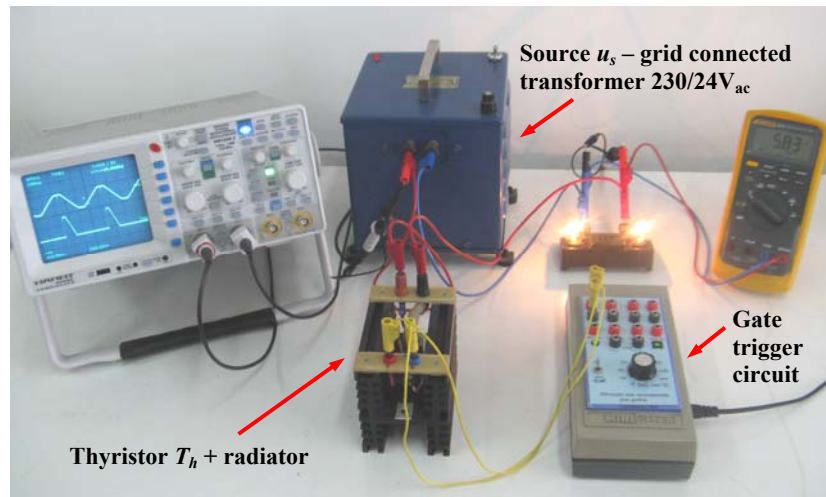


Fig.3.13 Image of the structure shown in Fig.3.4(a) with incandescent lamps as a load connected at the output of the half-wave rectifier.

References:

- [1] Mohan N., Undeland T., Robbins W., *Power Electronics: Converters, Applications and Design*, Third Edition, Published by John Willey & Sons Inc., USA, 2003.
- [2] Erickson R., Maksimovic D., *Fundamentals of Power Electronics*, University of Colorado, Boulder, Colorado, Published by Kluwer Academic Publishers, USA, 2001.
- [3] Albu M., *Electronică de putere - vol I: Noțiuni introductive, dispozitive, conversia statică alternativ-continuu a energiei electrice*, Casa de Editură “Venus” Iași, 2007.
- [4] Diaconescu M.P., Graur I.: *Convertoare statice – baze teoretice, elemente de proiectare, aplicații*, Ed. „Gh. Asachi”, Iași, 1996.
- [5] Ionescu Fl., Floricău D., Nițu S., Six J.P., Delarue Ph., Boguș C.: *Electronică de putere - convertoare statice*, Ed. Tehnică, București, 1998.
- [6] Kelemen A., Imecs M., *Electronică de putere*, Ed. Didactică și Pedagogică, București, 1983.
- [7] <http://pdf.datasheetcatalog.com/datasheet/Temic/mXyzurqş.pdf> - *Phase Control Circuit for Industrial Applications*