Lab no. 5

CONTROL OF THE POWER MOS GATE TRANSISTORS

1. Introduction

The MOS gate power devices are voltage-controlled switches because they have an isolated control terminal, integrated into a ***M**etal-**O**xide-**S**emiconductor* (MOS) structure. Taking into account their qualities (low control power, high switching frequency etc.), most of the recent researches have been focused on the development of these devices. Nowadays, we find on the market many types of MOS gate devices such as: power MOSFETs (MOS ***F**ield **E**ffect **T**ransistors*), ***I**nsulated **G**ate **B**ipolar **T**ransistors* (IGBTs)***, M**OS **C**ontrolled **T**hyristors* (MCTs) etc.

Since the power control of the MOS gate devices is negligible, the integrated control circuits, named ***MOS G**ate **D**rivers* (MGDs), can be used. These integrated drivers are complex, with multiple functions. They greatly simplify the structure of the power electronics systems, increase their operating performance and reduce them in size. With a great experience in the field of power semiconductor devices, some manufacturers have included the MGDs in modules with the MOS gate power devices. Thus, they have laid the foundations of the *smart power* technology which currently provides on the market many types of ***I**ntelligent **P**ower **M**odules* (IPMs) at an attractive price. Considering these advantages, coupled with its high speed quality, there is an explainable trend of increasingly use of the MOS gate power devices, in disadvantage of the GTOs or the power BJTs.

2. Symbols, semiconductor structure and static characteristics of the power MOSFETs

As the name suggests, the power MOSFET type transistor is the first representative of the MOS gate devices class. In Fig.5.1 are shown the symbol and the semiconductor structure of the most used power MOSFET, the *n*-channel transistor. The power terminals, called ***drain*** (D) and ***source*** (S), must be biased as in the figure, so that the device can operate as a unidirectional switch. The control voltage, labeled v_{GS}, is applied between the gate (G) and the source terminals. In the active on-state, the gate voltage value can control the current through the transistor, named drain current - i_D. If the power MOSFET is a n-channel transistor the gate voltage must be positive ($u_{GS}>0$) to obtain the device on-state.

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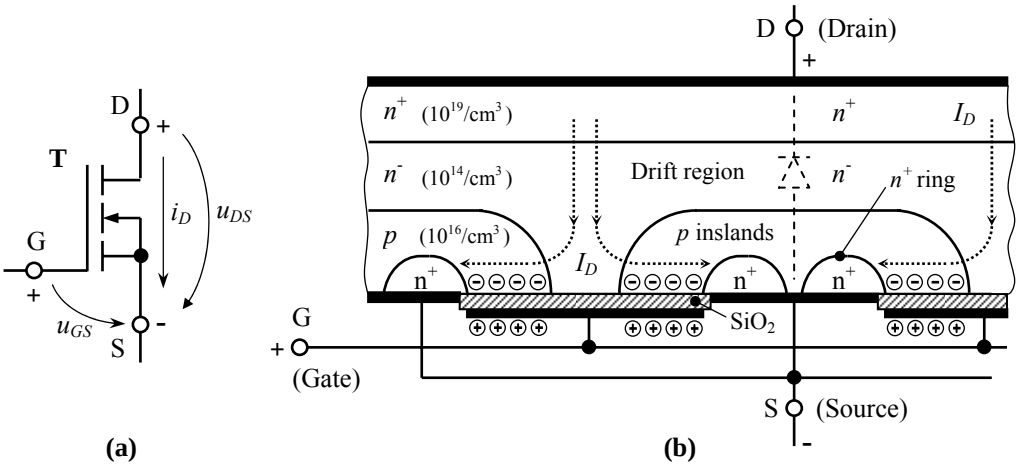

Fig. 5.1 The symbol (a) and the semiconductor structure (b) of a power *n*-channel MOSFET.

The vertical semiconductor structure of a power MOSFET contains four layers obtained by diffusion on a silicon disc - Fig.5.1 (b). The starting layer (substrate) is the drain layer (n^+) which covers the entire surface of the disc. Over this layer an epitaxially layer is grown, the drain drift region (n^-). As other power devices, the thickness of this layer depends on the rating voltage for which the transistor was designed. In the drift layer there are in-depth shaped, by diffusion, *p*-type islands (body channel regions) which form elementary MOS transistors. In every *p*-type island it is again shaped by diffusion a n^+ ring that is connected to the source terminal. The conduction channels appear on the surface of the semiconductor chip due to an electric field created by the gate (see the negative charges under the grid). Thus, the drain current I_D can flow radially, crossing the *p*-type circular bands, between the n^+ ring and the drift region surface that surround all of the *p* islands.

It can be seen in Fig.5.1(b) that the transistor remains in off-state, when it is forward biased, but the gate is not polarized. Basically, the n^+ layer in contact with the drain terminal, the drain drift region (n^-) and the *p* islands in contact with the source terminal form a parasitic power diode structure, reverse biased in this case. The forward blocking capability of the transistor is given by the reverse breakdown voltage of this diode, which in turn depends on the drift region's thickness. The same parasitic diode cancels the reverse blocking capability of the power MOSFETs. However, its presence is beneficial in most power structures because it can play the role of a recovery diode.

By gate polarization, which means a positive voltage applied between the gate and the source terminals ($u_{GS}>0$), the MOS capacity begins to charge as shown in Fig.5.1 (b). In this way, under the gate oxide (SiO_2) layer, on the surface of the *p*

circular bands, negative charges appear. If the gate voltage is low, below a threshold value ($u_{GS}<U_{GS(th)}$=2÷4V), these negative charges are obtained only due to a depletion process of the near *p* semiconductor material. Thus, the positive charges (holes) are rejected in depth and the negative charge of the MOS capacity is formed exclusively of acceptor ions. They cannot initiate the channel conduction and hence the transistor turn-on because these ions are immobile in the semiconductor crystal lattice.

If the gate voltage exceeds the transistor threshold value ($u_{GS} >U_{GS(th)}$) the so called ***inversion phenomenon*** occurs by which the *p*-type semiconductor under the gate isolating layer acquires the features of a *n*-type semiconductor that enriches with free electrons the negative charges of the MOS capacitance armature. Due to their mobility, the electrons create a bridge between the drift zone and the n^+ rings connected to the source terminal. Thus, the drain current start to flow through the path lines presented in Fig. 5.1(b). These bridges form an ensemble called the ***conduction channel*** of the MOSFET transistor, which in this case is of type *n* because it consists of negative charges (electrons). Once the drain current begins to flow, the electrons spread to the positive potential, created by the drain terminal in the drift zone. The continuous replacement of the electrons departed from the channel zone is achieved by the n^+ rings connected to the negative voltage of the source terminal.

The phenomenon in which the conductivity of a semiconductor material is modulated via a voltage or an electric field is called a ***field effect*** *and the transistor that uses it has been known as* ***F****ield* ***E****ffect* ***T****ransistor* (***FET***). These ones can be of many types. The MOSFET transistor achieves the field effect through the MOS capacitance as described above.

As presented above, due to the parasitical diode (n^+- n^-- p) that stands between the drain and the source terminals, the power MOSFET transistor cannot block the reversed voltages. For this reason, the volt-ampere static characteristics will be drawn only in the first quadrant of the *i*-*v* axis system. Thus, in the Fig.5.2(a) it is presented the transistor on-voltage (the drain-source voltage → u_{DS}) and the drain current (i_D) for different values of the control variable (u_{GS}).

If the gate voltage is zero or is under the threshold value $V_{GS(th)}$ (*gate-source threshold voltage*) the device remains in off-state and the operating point is placed on the *forward blocking characteristic* (i_D = 0) given that the drain-source voltage does not exceed a maximum limit. If the drain-source voltage exceeds the maximum value ($U_{DS} >U_{DS(max)}$) the transistor breakdowns and the drain current increases up to a value imposed by the external load circuit. Just like in the case of the power bipolar junction transistor, the forward breakdown voltage is labeled in the catalogue with the BV_{DSS} (***D****rain-****S****ource* ***B****reakdown* ***V****oltage, gate-source* ***S****hort circuited*) and it is given for the situation in which the control voltage is zero (the gate-source terminals are short-circuited).

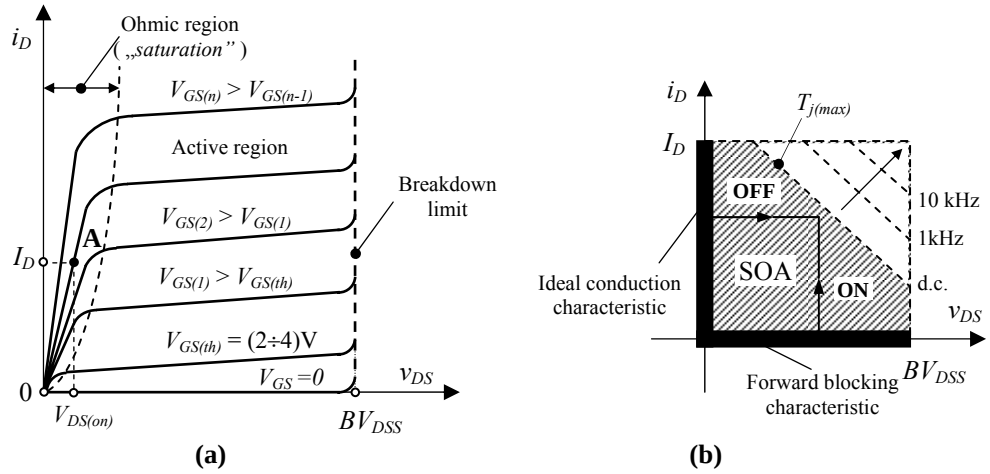

Fig. 5.2 (a) Real *i-v* static characteristics for a power MOSFET transistor;
(b) Idealized *i-v* static characteristics and the safe operating area (*SOA*).

The controlled turn-on of the MOSFET transistor occurs when the gate voltage exceeds the threshold value ($v_{GS} > V_{GS(th)}$). In Fig.5.2(a) more static characteristics for different gate voltage values are presented:

$$V_{GS(prag)} < V_{GS(1)} < V_{GS(2)} < ..... < V_{GS(n-1)} < V_{GS(n)} \le V_{GS(\max)} \qquad (5.1)$$

Due to the very small thickness of the isolating layer between the gate and the semiconductor, it is not permitted to use high gate-source voltages. It is estimated that values over (20÷30)V can breakdown the SiO_2 layer. For this reason, the manufacturing companies indicate a cautious manipulation of these devices, while the driver circuits cannot use control voltages higher than $V_{GS(\max)} = 20\text{V}$. To fully turn-on the MOSFET transistors, the gate voltage must be in the range of (10÷15)V. Usually, the standard value of V_{GS} is 15V.

Similar to all power transistor devices, even the static characteristics of the power MOSFET transistor have two operating regions:

- ***active region*** in which the value of the current through the transistor is controlled via the control variable (v_{GS}) and a significant voltage drop appears on the transistor;
- ***ohmic region*** in which the transistor is fully on, the voltage drop across the device ($U_{DS(on)}$) is low and little dependent on the drain current.

The designation of *ohmic region* wishes to emphasize the various processes that occur in the MOSFET type transistor when it is in on-state in contradiction with

the bipolar transistor where this state is included in the saturation region. In bipolar junction transistors the fully on-state is achieved through saturation with charge carriers of the base layer and of the collector's drift region, while in MOSFET transistors the same phenomenon is achieved by inducing a conduction channel that acts as a resistor with a very low value. However, taking into consideration the widespread of the term "*saturation*", it is used as well for the MOSFET transistor in various literatures.

The on-state power losses of the MOSFET transistors are defined by the product:

$$P_{on} = V_{DS(on)} \cdot I_D \tag{5.2}$$

in a steady-state operating point labeled A. On the other hand, starting from a resistive behavior of the MOSFET transistor, during the on-state the voltage drop on the device is given by the equation:

$$V_{DS(on)} = r_{DS(on)} \cdot I_D \tag{5.3}$$

where $r_{DS(on)}$ is the ***static drain-source on resistance*** which the drain current flows on the path shown in Fig. 5.1.(b). It is estimated that aproximatively 70% of the conduction power losses occur in the drift region. The resistance of that zone, as well as the resistance of the conduction channel, depends on the maximum voltage for which the power MOSFET transistor was made. Following the computations and the experiments, the literature indicates an approximate relation for the on-state transistor resistance:

$$r_{DS(on)} \approx k \cdot \left[U_{DS(\max)}\right]^{2,5} \tag{5.4}$$

The maximum drain current that can be sustained by a power MOSFET in a continuous mode, without thermal destruction, is labeled in various catalogues with I_D, and the maximum pulse current is labeled with I_{DM}. It has to be noted that due to the ***positive temperature coefficient***, the MOSFET power transistor cannot be destroyed through *thermal runaway* phenomenon, therefore it does not submit to the secondary breakdown process.

Even though the on-state voltage is relatively high for the MOSFETs, when the power structures with these devices are analyzed, the voltage drop across them can be neglected if the operating point is located inside the ohmic zone. Thus, it can be considered that this point is situated on the ideal conduction characteristic, as presented in Fig. 5.2(b). Also, taking into account the forward blocking characteristic and the fact that the switching from one characteristic to another can be made in both directions with the help of a control signal, one can obtain the features of an ideal unidirectional static switch.

The surface between the blocking characteristic, the conduction characteristic and the limits imposed by the maximum continuous current I_D, as well as the forward breakdown voltage BV_{DS}, forms the ***S**afe **O**perating **A**rea* (SOA) of the power MOSFET – Fig. 5.2(b). The shaded area represents the SOA corresponding to a continuous drain current. If the transistor operates in switch-mode with a certain switching frequency and with a duty ratio of the PWM control signal, the SOA can be extended.

3. Symbols, semiconductor structure and static characteristics of the IGBT transistors

If the BJTs characteristics are analyzed in comparison with the MOSFETs characteristics, as presented in the Tabel 5.1, one can see a perfect complementarity between the two controllable semiconductor devices.

Table 5.1 The complementary characteristics of the power BJTs and MOSFETs.

Device type	Conduction power losses	Switching power losses	Control power
BJTs	small	high	high
MOSFETs	high	small	small
IGBT	medium	medium	small

The power bipolar junction transistors present the saturation advantage, from which derives the low conduction power losses and the disadvantage of a slower dynamics which determines high switching power losses, as well as the necessity of an important control power. In comparison, the power MOSFETs have a relatively high conduction resistance which causes important conduction power losses and, in exchange, it is much faster (low switching power losses) and requires a negligible control power due to the MOS gate.

Starting from the upper observations, the researchers have tried to synthesize on the same silicon waffer a composed device that is able to assume the advantages of the power BJTs and those of the power MOSFETs. These efforts have lead to the creation of the ***I**nsulated **G**ate **B**ipolar **T**ransistor* (IGBT). It is obvious that the new device could not replicate exactly 100% the performances of the „parents" taking into account the saturation and the switching speeds.

The IGBT transistor was launched on the power semiconductor market in 1982. Fig.5.3 presents the symbol evolution for an IGBT with *n*-type channel. The first symbol - see Fig.5.3(a) - was used mainly at the beginning and shows the transistor as a

MOSFET. The main difference from the *n* channel MOSFET symbol is that it has a second arrow whose head points the direction of the charge injections from the supplementary p^+ layer. If this symbol is used, the power terminals will be called *drain* (D) and *source* (S) and the current that flows through the transistor is called *drain current* (i_D). The symbols from Fig.5.3.(b) and (c) represent the IGBT as a MOS structure in the control side and as a bipolar structure in the power side. If these symbols are used, the power terminals will be called *collector* (C) and *emitter* (E), while the current flowing through the transistor will be the *collector current* (i_C). All the symbols have the control terminal labeled with G (*gate*).

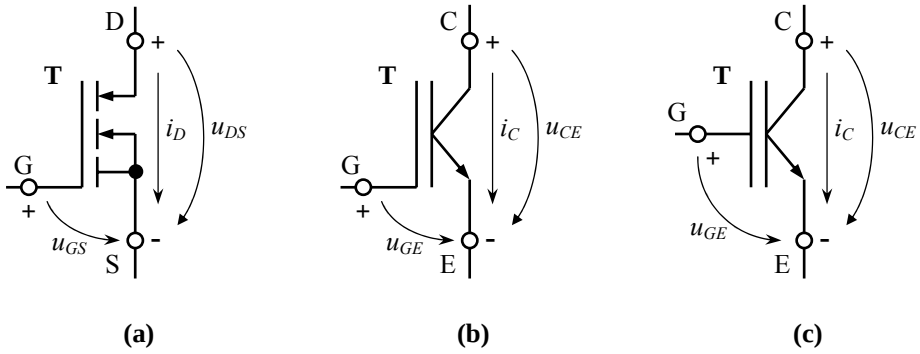

Fig. 5.3 Various symbols for an IGBT with *n*-type canal.

Since it was launched on the market, the IGBT had a powerful ascent, being preferred in many applications. The IGBT is a real "locomotive" for the power electronics, causing an unprecedented development in this domain, both by simplifying the power structures and by increasing the conversion quality. Today, the new IGBT generations built in *trench* structures can obtain the performances in voltage and current up to 6.5kV and 2500A, comparable to the GTO's which had the upper hand at these features. Also, taking into account the high switching frequency and the ease control, one can explain the designers' and the users' preference for this type of power semiconductor device.

The semiconductor structure of the IGBTs is almost identical with the semiconductor structure of the power MOSFETs. For example, the only element that differentiates the *n* channel IGBT from a MOSFET having the same channel is the p^+ supplementary layer, also called ***injection layer***, placed on the side of the drain over the n^+ layer, as shown in Fig. 5.4. The role of the p^+ supplementary layer is to provide minority carriers (holes – positive charges) which will be injected in the (n^-) drift zone in order to increase its conductivity. On the other hand, in the drift zone arrive electrons (negative charges) from the emitter (source) terminal, electrons which follow the channel conduction path induced by the field effect. Thus, the current through the IGBT has a bipolar characteristic because it appears after the simultaneous

displacement of the positive and negative charges which meet and partially neutralize each other in the drift zone.

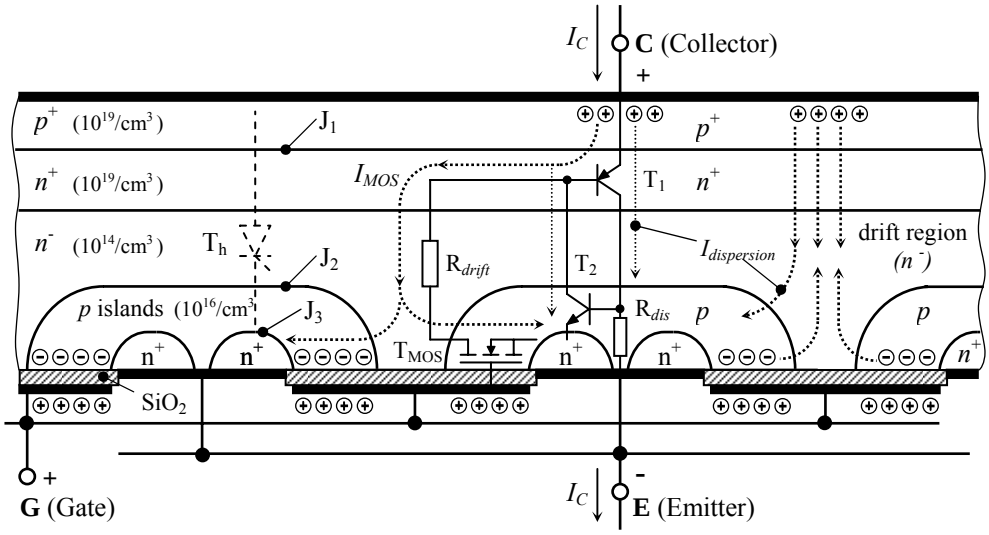

Fig. 5.4 The semiconductor structure of a planar IGBT with *n*-type canal

The conductivity modulation of the drift zone through which the static on resistance is substantially decreased and the bipolar character of the transistor current differentiates the IGBT from the power MOSFET. In a power MOSFET the voltage drop on the drift region dominates the conduction power losses and by decreasing the drift resistance inside an IGBT will significantly increase their loading capacity.

When the IGBT is in off-state, the C-E forward voltage (u_{CE}>0) is sustained by the J_2 (n^--p) junction, reverse biased. If the doping level and the thickness of the drift region (n^-) are well optimized, so that, when the transistor is forward biased with maximum catalogue voltage, the depletion layer from this region does not reach its border, the ***n*$^+$** *buffer layer* may be missing. Thus, one can obtain the ***symmetric IGBT***, also called ***N*on *P*unch *T*hrough** IGBT (**NPT-IGBT**). Besides the advantages of simplifying the semiconductor structure and therefore the fabrication process, the symmetric IGBT brings as well the advantage of blocking high reverse voltages. It is a feature that misses in the case of the bipolar transistors as well as in the case of the power MOSFET transistors, whence the possibility for the NPT-IGBTs to be used in AC applications. The blocking capacity of the reverse voltages is achieved via the transformation of the J_1 junction from a p^+-n^+ junction to a p^+-n^- junction which can sustains high reverse voltages. Thus, the drift region plays a blocking role, not only for forward voltages, but also for reverse voltages applied to the IGBTs.

On the other hand, *by the presence of the* $\boldsymbol{n^+}$ *buffer layer* with an optimum thickness and a well chosen dope level, one can derive the following advantages for an IGBT transistor:

- diminishing of the on-state voltage;
- shortening of the transistor's blocking time.

The IGBTs whose structure includes the n^+ buffer layer is called ***asymmetric IGBTs*** or ***P**unch **T**hrough IGBTs* (**PT-IGBTs**). Their disadvantage is mainly in the significative reduction of the reverse blocking capacity due to the low breakdown voltage of the J_1 junction that has both layers heavily doped (p^+- n^+).

As it can be observed in Fig. 5.4, the complete equivalent scheme of an IGBT includes a MOSFET transistor (T_{MOS}) and two bipolar junction transistors (T_1, T_2) – Fig.5.5(a).

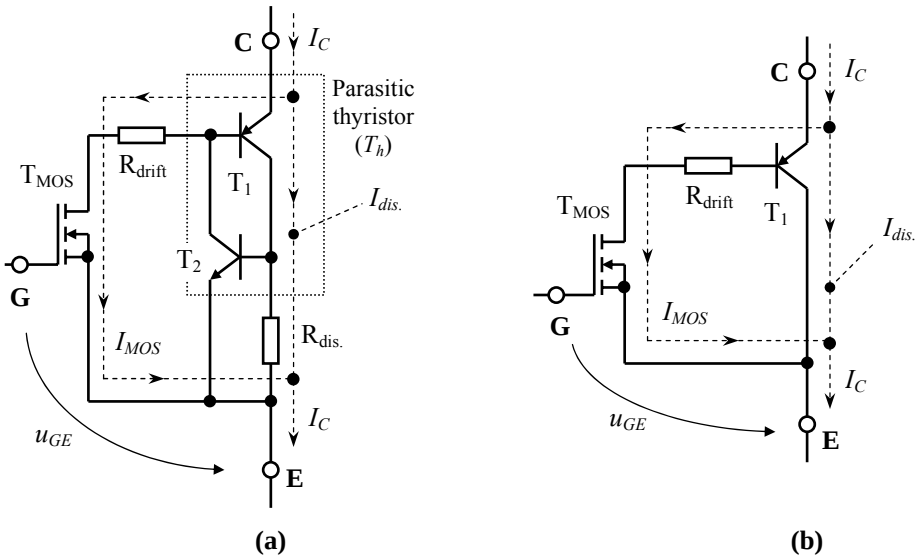

Fig. 5.5 Equivalent schemes of an IGBT: (a) complete form; (b) simplified form.

It can be seen in Fig.5.5(a) the existence of a T_h parasitical thyristor suggested by the connecting mode of the two bipolar transistors T_1 and T_2 . If sufficient measures are taken to avoid the parasitical thyristor turn-on (avoid the IGBT ***latching phenomenon***), one can ignore the T_2 bipolar transistor and the R_{dis} lateral dispersion resistance. Thus, results the equivalent simplified scheme of the IGBT, as presented in Fig. 5.5(b). This one equates the IGBT with a Darlington configuration formed by a MOSFET having the driver role and by a power BJT. In reality, the T_{MOS} transistor is equivalent with an important number of MOSFET micro-transistors connected in parallel, all contributing to the base current control of the T_1 main transistor of *pnp* type.

A significant increase of the IGBT collector current was achieved by modifying the manufacturing technology which augmented significantly the density of the elementary IGBT transistors inside a silicon chip. The new technology abandons the planar semiconductor structure and use a new ***trench*** structure. This consists in modifying the position of the inversion layer from the surface of the silicon chip on a perpendicular direction in the depth of the semiconductor material. Fig 5.6 shows the way in which the MOS cells are reconfigured in the trench structure, by building the gate terminals like trenches that cross the body of the *p* channels.

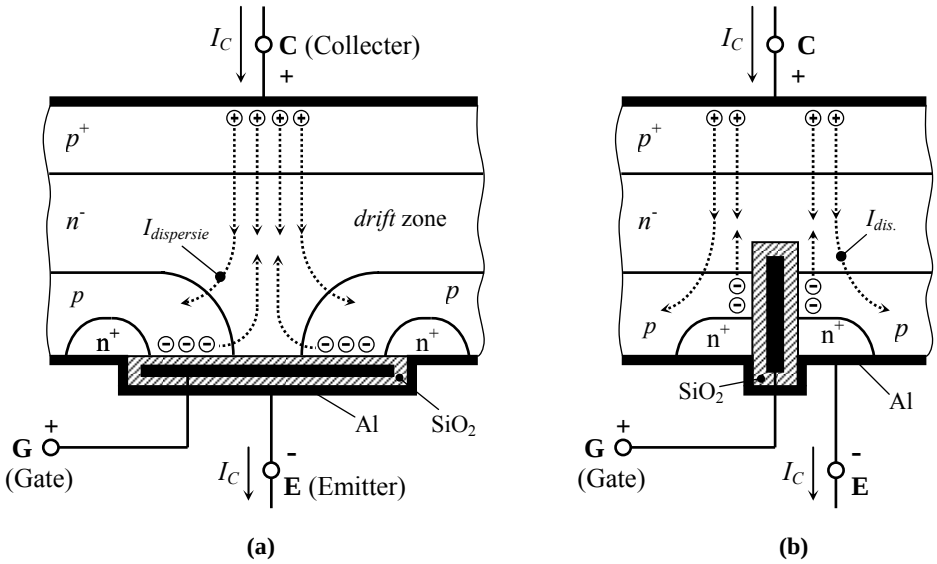

Fig. 5.6 The planar type semiconductor structure (a) in comparison with the trench type one (b) of a symmetric IGBT.

A NPT-IGBT with a trench structure from the third generation can take a current that is 50% higher than a NPT-IGBT with a planary structure from the second generation having the same silicon chip. This gain is explained through a superior valorization of the semiconductor material section and through uniformization of the current density on the cross section of the silicon chip.

The control and operating mechanism of the semiconductor structure is similar to that described at the power MOSFET. The direct and reverse blocking is assured by the J_2 and J_1 junctions.

The *i-v* static characteristics of the IGBTs are similar to those of the power MOSFETs shown in Fig.5.2 with the specification that the denominations of the power terminals are others and the symmetric IGBT has the reverse blocking capacity. Thus, in Fig.5.7(a) the $v_{CE} = f(i_C)$ static characteristics are shown for such a transistor (NPT-IGBT). If an asymmetric IGBT transistor is used (PT-IGBT), only the first

quadrant of the v_{CE} - i_C plan will be considered. In fig 5.7(b) are presented the ideal characteristics and the safe operating area in the case of the transistor forward biased.

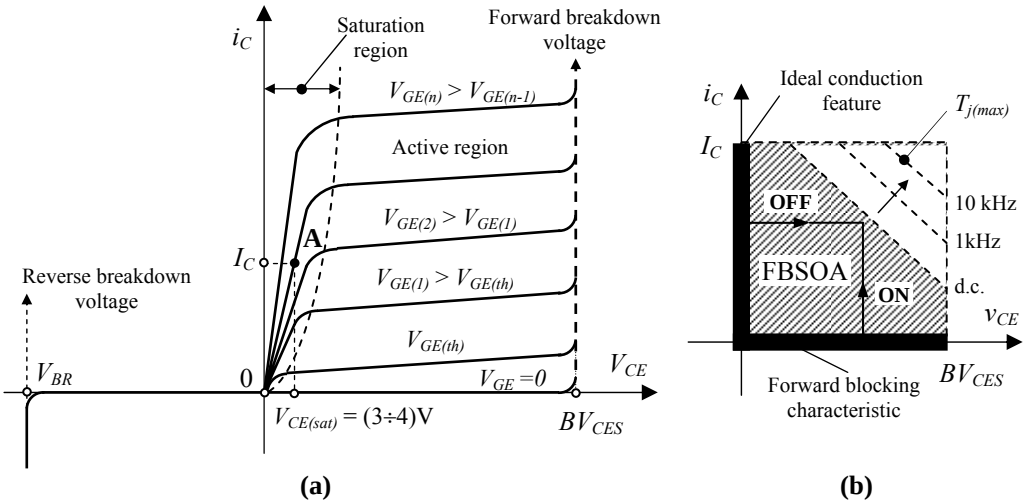

Fig. 5.7 (a) The real *i-v* characteristics for an IGBT; (b) The ideal *i-v* characteristics and the ***F**orward **B**ias **S**afe **O**perating **A**rea* (*FBSOA*).

If a symmetrical IGBT is reverse biased ($u_{CE} < 0$), the collected current (i_C) is zero as long as the voltage is maintained under the reverse breakdown value V_{BR}. Once this value is exceeded, the phenomenon of the reverse breakdown appears which can lead to the device's destruction. For this reason one must take care in the AC applications to use reverse voltages which do not exceed the maximum catalogue value - V_{RRM} (***M**aximum **R**epetitiv **R**everse **V**oltage*). In the power structures supplied with DC voltages, the IGBT are provided with recovery diodes which exclude the occurrence of reversed voltages on the device. For these applications it is not necessary to use NPT-IGBTs.

If the IGBT is forward biased and it is not controlled with an appropriate gate voltage ($V_{GE} < V_{GE(th)}$), the operating point is placed on the forward blocking characteristic (I_C =0). If the C-E voltage (V_{CE}) exceeds the BV_{CES} (***C**ollector–**E**mitter **B**reakdown **V**oltage, gate-emitter **S**hort circuited*) the forward breakdown appears and the collector current increases up to the value limited by the external circuit. The uncontrolled turn-on must be avoided, because transient processes may appear in the semiconductor structure that can destroy the device.

The IGBT controlled turn-on is obtained when the gate voltage exceeds the threshold value ($V_{GE} > V_{GE(th)} > 0$). Fig.5.7(a) shows more *i-v* characteristics for the different values of the gate voltage in a range recommended by the manufacturer:

$$V_{GE(th)} < V_{GE(1)} < V_{GE(2)} < ..... < V_{GE(n-1)} < V_{GE(n)} \le V_{GE(\max)} \qquad (5.5)$$

As in the case of a power MOSFETs, due to the low thickness of the isolated layer (SiO_2) between the gate and the semiconductor, there are not permitted gate-emitter voltages beyond $U_{GS(\max)} = 20\text{V}$. For the IGBT turn-on it should be used the standard gate voltage of the MOS gate devices, the value of 15V. This value ensures the flow of a collector current of up to 10 times higher than the rated current, without the transistor having to enter in the active region.

The voltage drop on the saturated IGBT transistors can be neglected in the analysis of the power structures which operate with voltages around hundreds or thousands of volts. Consequently, one can consider that the operating point A can be placed on an ideal conduction characteristic, as presented in the Fig.5.7(b). The denomination of saturation region wishes to emphasize the fact that the conduction process in an IGBT has a bipolar character, although the semiconductor structure resembles more with that of a power MOSFET transistor. Moreover, the denomination is justified also by the modern symbol of IGBT which regards the power side as a bipolar transistor for which a specific terminology has to be used.

The conduction characteristic is limited by the maximum collector current that an IGBT is able to sustain continuously without thermal damages. This current is labeled with I_{CM} and it is a catalogue parameter. The IGBT has an almost ***neutral temperature coefficient*** (significant changes of the $V_{CE(sat)}$ voltage do not occur along with the increase of the semiconductor's temperature). From this point of view, the IGBT is a very robust device able to withstand short-circuit currents. This special feature is confirmed by the manufacturing companies and the numerous research laboratories, as well as in the catalogues and scientific articles. Based on these, one can say that the IGBT is able to withstand important short-circuit currents without suffering thermal destructions for a time of (7÷ 10) μsec.

In Fig. 5.7(b) is presented the ***F**orward **B**ias **S**afe **O**perating **A**rea* (FBSOA) when the IGBT is forward biased. There are rare cases in which the symmetric IGBT's operate in AC applications, when the IGBT is reverse biased. The FBSOA is the shaded surface contained between the blocking characteristic, the conduction characteristic and the limits imposed by the I_{CM} maximum current, respectively the BV_{CE} forward breakdown voltage. As in the MOSFET transistor case, if the transistor operates in switch-mode with a certain switching frequency and with a duty ratio of the PWM control signal, the FBSOA can be extended.

4. Overview of power MOS gate transistors control

Power semiconductor devices with MOS gate have the control terminal electrically isolated by the semiconductor structure through a thin oxide (SiO_2) layer. All these devices are voltage controlled. The gate voltage controls the *field effects* based on which the device is turned on.

Voltage control of the MOS gate devices ***doesn't*** *suppose only a simple bias of the gate terminal, without any power consumption.* Metal-oxide-semiconductor combination is actually an equivalent capacitor that must be charged first to achieve a certain level of voltage on the gate. This consists in bringing a certain amount of electrical charge on the metal armature of the gate, fact that can be achieved through an electric current. For this reason the gate current exists only during transient time intervals of turn-on or turn-off, in the remaining on-state time interval the gate current is zero, so no control power is consumed. If we take into consideration that the value of equivalent gate capacity is low (hundreds pF÷nF) and the control voltage is around 15V results a negligible energy consumption in one switching period. For a switching frequency of kHz order in a second the control power is below 1mW. At the entire control circuit level, even for high switching frequencies of hundreds of kHz, the power consumption is no more than hundreds of mW.

Control circuits for the MOS gate transistors are called ***MOS Gate Drivers*** (MGDs) or can be shortly called as ***drivers***, name used also for the control circuits of power BJTs. The specific functions are also the same, indicating that, since the drivers for MOS gate transistors are made in the most of the cases as integrated circuits, their functions have been developed with additional extensions and smart features.

To control a n-channel MOS gate transistor, it is required a positive gate voltage of +(10÷15)V for the turn-on and a negative voltage of -(5÷15)V for the device turn-off. These control voltages must exist during all the on-state or off-state time intervals. As discussed in the previously paragraphs, for the fully on-state is recommended the standard gate voltage of +15V. Theoretically, to obtain the device off-state is sufficient a near zero value for the gate voltage, below the threshold value: $U_{GS(th)}$ ($U_{GE(th)}$) = (2÷4)V. In practice, it's preferred a negative voltage, high enough, to reject any interference voltages induced in the connecting wires between the control circuit and power device. For safety the wires should be always twisted.

Depending on the speed with which the gate capacity is charged and discharged it can be adjusted the turn-on or turn-off speed, respectively. For this reason an important parameter of the *driver* is the time constant of the gate circuit. Since the gate MOS capacitance is already fixed, it follows that the parameter on which we can adjust the time constant is the gate resistance of the control circuit. Thus, ***through a gate resistor R_G we can set the maximum amplitude of the gate current and the time intervals of the transient states (turn-on and turn-off).***

For choosing the gate resistance value it should be optimized the following conflicting requirements:

- Choosing a gate resistance as small as possible to minimize the transient time in order to decrease the switching power losses and increase the maximum switching frequency of the power MOS gate device.

- Increasing the gate resistance to a certain value for which the peak of the gate current $\hat{I}_G$ does not exceed the maximum capacity of the low-power transistors from the output stage of the driver.
- Limit the gate resistance to the minimum so that the slopes of the power current through the transistor does not exceed the maximum value of the catalogue: $di/dt<(di/dt)_{max}$.
- Choosing the gate resistance so that, when the transistor is turned-off, the decrease slope of the power current does not cause high switching overvoltages in order to eliminate the *dv/dt* snubber circuit.

Regarding to the above requirements should be made some clarifications. Firstly, at high power devices (IGBTs), due to the large gate capacities, significant gate currents are needed to obtain reasonable switching times. For the IGBTs with rated voltages over 1000V and rated currents over hundreds of amperes, gate current pulses having $\hat{I}_G = (7 \div 15)\text{A}$ amplitude are necessary. In order to sustain such repetitive peak currents, the integrated driver must be completed with an external final amplifier stage. If the supply voltage of the driver is around 15V the gate resistor has the value of (2÷3)Ω and it is non-inductive to obtain a step response.

Secondly, ***to control separately the turn-on and turn-off transition times we use different gate resistances*** $\boldsymbol{R_{G(on)}}$, $\boldsymbol{R_{G(off)}}$. At the transistor's turn-on no special restrictions are imposed, therefore the gate resistance $R_{G(on)}$ will be chosen taking into account the objective to minimize the turn-on transition time and to limit the on peak gate current. The gate resistance $R_{G(off)}$ will be chosen more carefully taking into account also the current slope optimization during turn-off time interval.

5. Functional structures of the MOS gate drivers (MGDs)

In a modern version, the MGDs are made with integrated circuits or specialized modules. On the other hand, no matter how complete could be these integrated drivers, they can't operate always alone, without any additional circuit elements, since the integrated drivers are designed to operate with certain parameters (maximum gate currents, time response to the overcurrents occur, clock frequencies etc.). On the other hand, depending on the type of the integrated driver and on the application performances, can be also added other block circuits such as: amplification stages, logic circuits, fault capture circuits, electrical isolation and communication circuits, START/STOP circuits, DC sources, etc. All of them are achieved with discrete circuit components such as: low-power transistors, analog or digital integrated circuits, optocouplers, resistors, capacitors, pulse transformers, etc.

Next will be presented, in a general form, some typically circuits used by the MGDs to understand more easily their functional structure, as well as the operation and use of these specialized integrated drivers.

a) The final stages of the MOS gate drivers

Fig.5.8 shows two final stages of a MGD. The symbolic switches K_{on} and K_{off} can be part of an integrated MGD or can be included in a separate, external, stage to get the current amplification. For practical reason, an IGBT was chosen as a representative MOS gate power transistor because it has a simpler symbol and it is one of the most used devices in the modern power electronics.

Fig.5.8(a) presents the final stage of a MGD that uses only one gate resistance R_G. Through the value of this resistance it's adjusted simultaneously both the turn-on and turn-off transition times. The switches K_{on} and K_{off} are low-power transistors which can be of a bipolar type or a MOSFET type, individual or in Darlington configuration. Usually, there are used complementary transistors connected in a *totem-pole* structure, as shown in Fig.5.9. According to the information presented above, these low-power transistors have to sustain the current pulses. If the final stage is included into an integrated MGD its catalog specification provides the maximum peak current ($\hat{I}_{\max}$) that it can provide. Depending on this parameter and on the voltage gate value (V_{G+}) it will be calculated the low limit of the gate resistance:

$$R_{G(\min)} = V_{G+} / \hat{I}_{\max} \tag{5.6}$$

If the final stage is a current amplifier that must be achieved separately from the integrated driver, the T_{on} and T_{off} transistors will be chosen depending on the repetitive current pulses required by the power MOS gate device to obtain the specify catalog switching times.

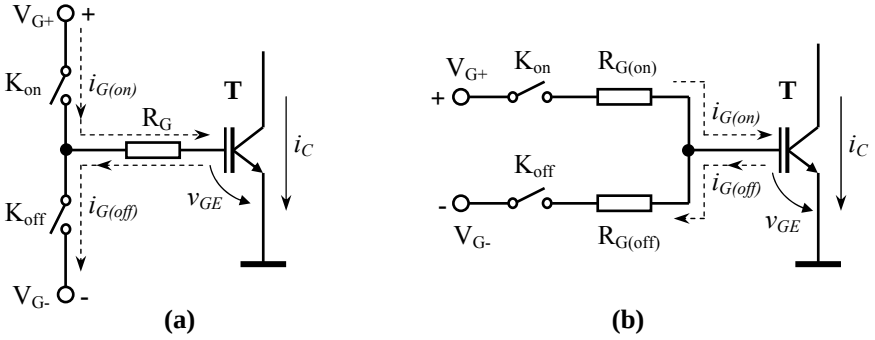

Fig. 5.8 Variants of some final stages of the MOS gate drivers: (a) with only one gate resistance; (b) with different gate resistances for turn-on and turn-off.

Fig.5.8 (b) shows a final stage with two distinct gate resistance $R_{G(on)}$ and $R_{G(off)}$. This configuration can be also implemented inside the integrated MGDs or can be achieved separately, as an additional amplification stage. In this last case the *totem-pole* structure formed with the two complementary low-power bipolar transistors can be used in different variants as in Fig.5.9.

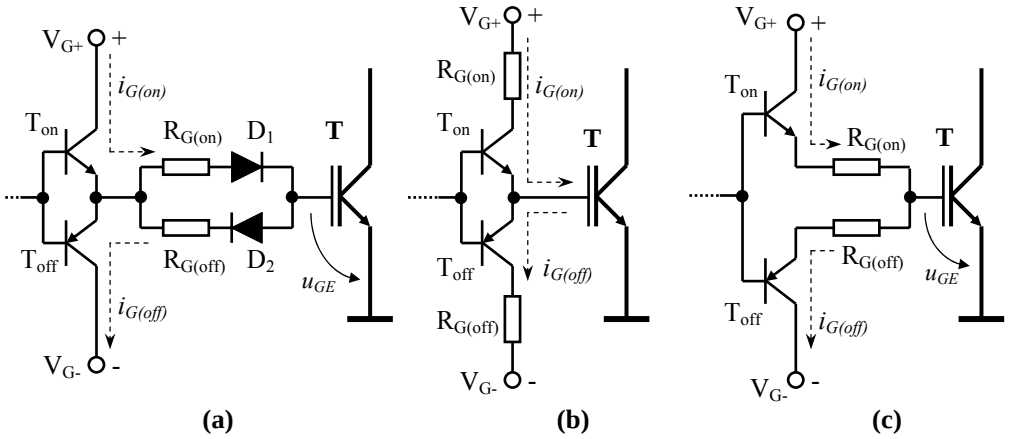

Fig.5.9 Final stage variants of the MGD circuits with two gate resistors.

Through the different gate resistors can be controlled separately the turn-on and turn-off switching times of the power MOS gate transistor. The choice for the values of the $R_{G(on)}$ and $R_{G(off}$ will be made taking into account the criteria presented in previous section.

b) <u>Protection circuits</u>

To implement the overcurrents' protection function, the integrated drivers include comparators with the help of which can be monitored the voltage drop on the shunt resistor connected in series with the power transistor or the voltage drop on the power transistor in on-state (V_{on}). Fig.5.10 presents a protection circuit that uses the desaturation effect of the transistor to sense a short circuit current. It is a modern and advantageous method because it excludes sensors or current transducers which are expensive and complicate the driver. In the MGDs catalogs this protection method is referred as ***DESAT protection*** (desaturation protection).

The main element that decides the power transistors turn-off is the comparator. At its inverting input terminal it is applied a reference voltage V_{ref} with the value range of (7÷15)V. At the noninverting input terminal it is applied an electrical potential given by the voltage across the on-state transistor ($v_{CE}=V_{on}$) and a small voltage given by the D diode: $V_{on} + V_D$. When the current through the transistor exceeds a maximum value ($i_C > I_{CM}$) the power device leaves the saturation region entering in the active region. This phenomenon called desaturation causes an increase of the V_{on} voltage that determines the comparator to switch.

After the comparator switching, the transistor T_1 is turned on and decreases the voltage gate (u_{GE}) to a value given by the D_z Zener diode, preparing the power transistor for turn-off. If the voltage across the transistor (u_{CE}) remains high for a certain time interval that excludes the possibility of a transient perturbation, the delay

circuit decides the power transistor turn-off through the T_2 turn-on that connects the gate to the ground (GND).

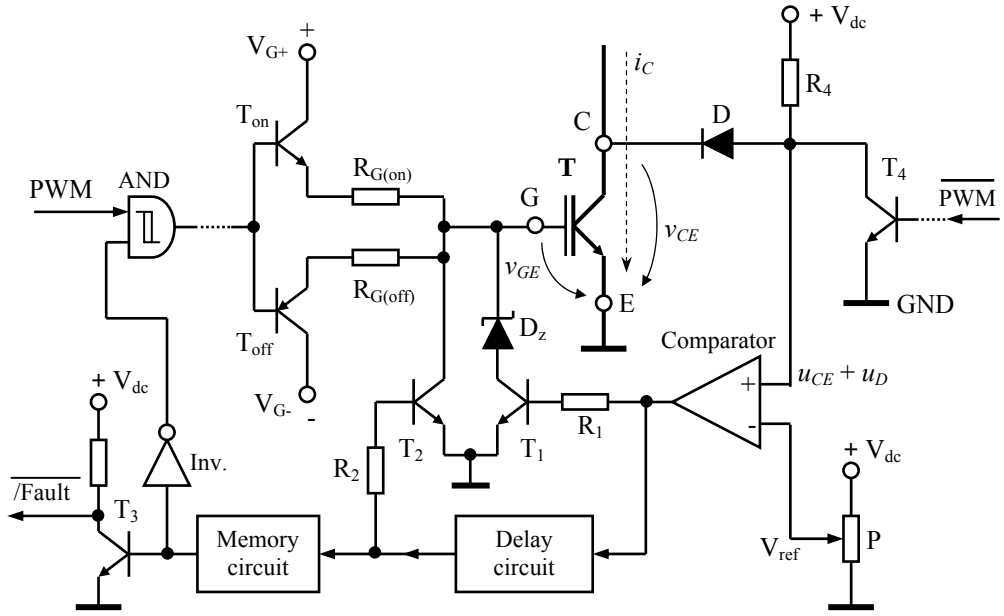

Fig. 5.10 Protection structure against the short circuit currents that uses the power transistor desaturation effect.

Some drivers are provided with the fault memory circuits. These ones can detect and sum many fault situations (overcurrents through the power transistor, supply voltages decrease - ***u**nder**v**oltages **l**look**o**ut-UVLO,* etc.), memorize these situations and turn-off the power transistor for an undefined time interval until it is turned on by a human operator. In the diagram of Fig.5.10 the memory circuit blocks the PWM control signal with the help of a logic AND circuit. In the same time, the memory circuit turn-on the T_3 transistor that decrease its collector potential to 0L (logic) that corresponds to the fault signal activation. In the case of the integrated drivers, this internal transistor provides an fault output of *open collector* type, a fact that allows a parallel connection of these ones into an OR logic circuit that can sum other fault signals coming from other MGDs.

There are integrated drivers that can memorize the fault situation and turn-off the power transistor only in a single (actual) switching period. At the beginning of the next time period the memory circuit is reseted by the PWM signal. For these drivers it is indicated to make an external latch circuit to capture the fault situation, because a repeated transistor turn-on in case of a short circuit could lead to a thermal destruction of the power device.

It should be noted that the protection circuit shall monitor the voltage drop across the power transistor just during the on time interval. Otherwise, during the off time interval the voltage across the transistor is normally high, which correspond to a false fault situation. This is why the integrated drivers activate the overcurrent protection after the turn-on signal was sent. In Fig.5.10 this feature is implemented with the help of the transistor T_4 whose state is controlled by the negated PWM signal ($\overline{PWM}$). So, when the power device is turned off, the transistor T_4 connects the noninverting input of the comparator to the ground. If the transistor T_4 is missing, on the noninverting input is applied the supply voltage $+V_{dc}$ because the diode D is reverse biased by the high voltage of the power source. Regarding this aspect, the reverse breakdown voltage of the D diode must be correlated with the voltage value of the power source. Also, the diode D must be fast, their switching times intervals must correspond to the requirements of the protection circuit.

Another important aspect that must be taken into consideration when the protection circuit is designed, is the transistor turn-off speed in the case of a short circuit. When a high current through the power transistor occurs, a fast turn-off determines a high *di/dt* and consequently high commutation voltages which can lead to the power transistor breakdown. Because of this, in short circuit conditions, the transistor turn-off must be done more slowly than in normal conditions. This turn-off technique is implemented in the block diagram of Fig.5.10 that presents a protection circuit for short circuit currents which operates in two consecutive steps. In the first step, the gate voltage is decreased bringing the power transistor state near the boundary between the saturation region and the active region, then in the second step the gate voltage is decreased to the GND level (0V).

The overcurrents' protection can be implemented also using current sensors. The less expensive option consists in using a shunt resistance connected in series with a power transistor or with a structure of many such devices. Simultaneous protection of a transistors group is usually used for H or three-phase bridges supplied with DC voltages.

The voltage drop across the shunt must be exactly proportional with the current value through the device ($v_{shunt} = R_{shunt} \cdot i_C$). For this, the sensor must be non-inductive. In addition, it must be calibrated with a high precision and must have a low resistance, of order (0.01÷0.1)Ω, to avoid important ohmic (Joule) losses. These strict features can be obtained through the complex and controlled manufacturing processes. It is necessary to use shunts from the professional companies which are called LVR (***L**ow **V**oltage **R**esistance*). The low resistance value allows using these shunts for currents of tens of amperes. For high currents of hundreds of amperes it is recommended to use fast current transducers (eg. Hall transducers) avoiding in this way an increased shunt power, over 10÷15W. In order to effectively dissipate the power converted into heat, some LVR resistances are designed to be mounted on the radiators, ensuring the electrical isolation with them.

c) Interface and isolation circuits

Usually, the power electronic converters or the power electronic systems contain a power part (structure) and a control part (block). Through the power structure flows the main flux of energy and it operates with high voltages and currents which generate important electromagnetic interferences. The control block operates with low signals, logic or analogic. The drivers are on the border between the two sides. The communication is done in both directions through logical signals. Therefore, the MGDs must contain a logic block capable to analyze and transform these logic signals and an interface block that can accomplish one ore more of the following functions:

- receiving logic control signals from the hierarchic superior block circuit, reshaping those in case they are affected by disturbances and adapting to the required logic level of the driver inputs;
- sending some feed-back logic signals which are communicated in the reverse direction for different situations or states reported by the control circuit;
- achieving the electrical isolation between driver and the digital control system.

Not always the integrated drivers can accomplish the isolation function. Fig.5.11 shows the block diagram of such a driver where we can see an interface circuit block without electrical isolation. If a logic level adaptation is necessary between the signals received from the microcontroller and the driver logic block, a different voltage is required to supply the interface block circuit. This voltage (V_{dc2}) must have the same amplitude as the logic signals (eg. the TTL logic level).

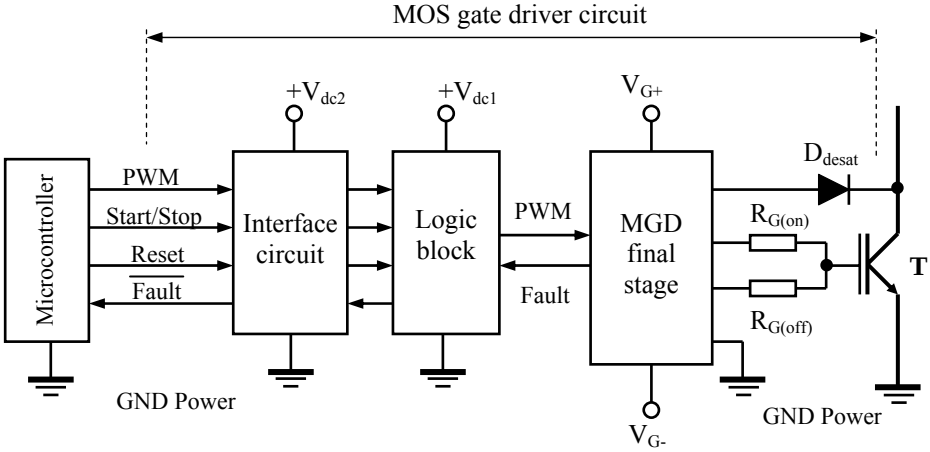

Fig. 5.11 The interface circuit placed in a MGD block diagram.
(represented here without electrical isolation)

The isolation elements like optocouplers or signal transformers can be placed at the input of the MGD or before the final stage. In Fig.5.12 it is presented the first variant in which the isolation circuit (an optocoupler) is located at the driver's input, where it interfaces with the digital control system (microprocessor - μP).

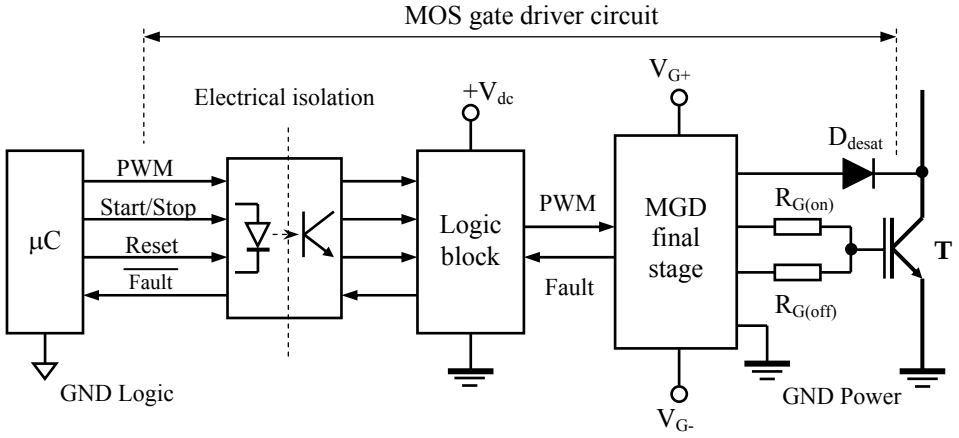

Fig. 5.12 The electrical isolation circuit (optocoupler) placed at the MGD's input.

In Fig.5.13 it is presented the second variant in which the isolation circuit (a signal transformer) is placed inside the driver, before the final stage and the protection circuit which are connected to the power structure fed with high voltages.

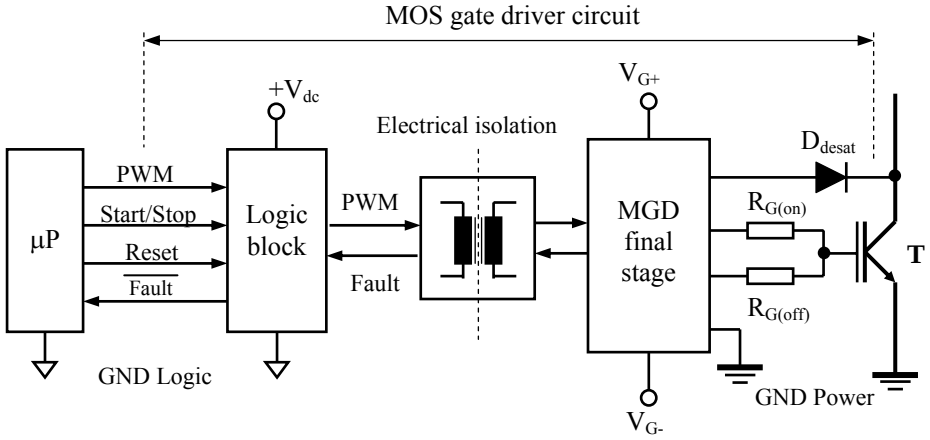

Fig. 5.13 The electric isolation circuit (signal transformer) placed inside the MGD.

d) Supplying variants of the MGDs

Another important aspect that must be taken into consideration when we design a MGD consists in choosing the supplying variant of the driver. For example,

the MGD shown in Fig.5.14 can operate if it is supplied with four different voltages: V_{dc1}, V_{dc2}, V_{G+} and V_{G-}. A solution to simplify this problem is to supply with the same positive voltages the logic block and the final stage ($V_{dc1} = V_{G+}$). Consequently, one must cancel the electrical isolation between the two stages and it must optimize the voltage level for a good operation of the both parts. Not always can we find solutions in this way because a complex driver circuit requires certain standard voltages for the logic circuits and other values for the gate voltages. For example, to get an effective value of +15V on the MOS gate, the V_{G+} voltage should be slightly higher to compensate the voltage drop across the T_{on} when it is in on-state:

$$V_{G+} = V_{GE(T)} + V_{CE(Ton)} = +(16 \div 18)\text{V} \tag{5.7}$$

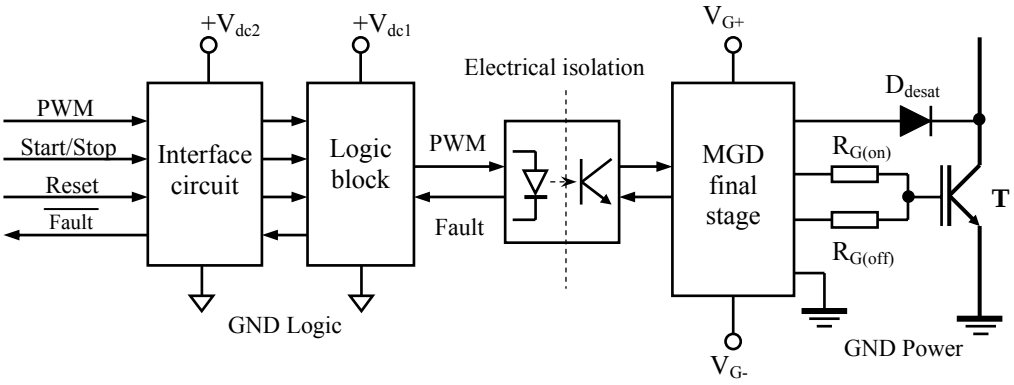

Fig. 5.14 Supply variant of a complex MOS gate driver.

The negative gate voltage required for transistor turn-off, will be chosen according to disturbances in the system and as shown above, it can take values in the range of:

$$V_{G-} = -(5 \div 15)\text{V} \tag{5.8}$$

If the electrical isolation is made before the final stage, the gate voltages (V_{G+}, V_{G-}) must come from a DC source that provides these voltages isolated from the voltages which supply the other blocks of the driver - Fig.5.13.

Also, in the logic side of the driver, many supply voltages may be necessary. It is possible that an integrated driver requires a supply voltage of V_{dc1} = +15V and the interface circuit together with the external digital system (μC) to operate with a supply voltage of V_{dc2} = +5V (TTL level).

From the above, it follows that to solve the problem of a single driver supply it is necessary to have two isolated DC sources, of which at least one must be able to provide more voltages. The problem is further complicated if the power structure contains several power transistors. Some of these transistors have the control terminal connecting to the *floating grounds* (GND_f).

To solve the problem of the DC sources for the complex control circuits, two options are available for the designer:

- Using a multiple-outputs regulated DC source with more electrical isolated outputs. This source can be linear and includes a line transformer with multiple, isolated secondary windings. It's a classical solution which has the disadvantages of great size, weight and low efficiency. The modern alternative is to use a multiple-outputs switch-mode DC source that eliminates the disadvantages of the linear sources.
- Using the integrated MGDs specially designed to reduce the number of sources or supply voltages (see *Semikron* SKHI modules).

6. Laboratory application

For the laboratory study of practical aspects related to control of a single power MOS gate transistor it will be done a laboratory setup whose image is shown in Fig.5.15 and whose block diagram is shown in Fig.5.16.

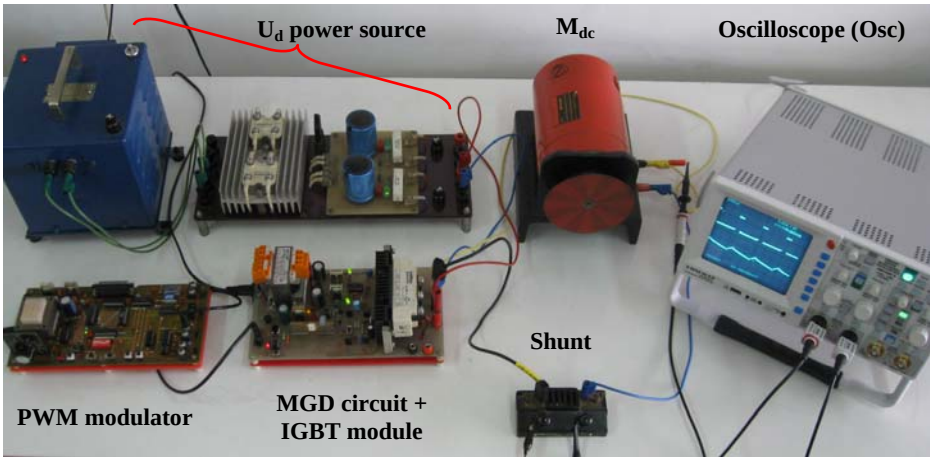

Fig. 5.15 Laboratory application image.

The laboratory setup comprises as the main element a board, a printed circuit that includes a multiple-outputs regulated DC source, a power semiconductor module and a MOS gate control circuit consisting of two distinct drivers. The image of this printed circuit designed and made as an application project in the power electronics laboratory is shown in Fig.5.17. The first driver circuit is achieved with discrete components (transistors, diodes, resistors, capacitors, etc.), while the second driver is designed with the HCPL 316J integrated driver. Both were made on the same board to highlight the difficulty of implementing a driver with discrete components compared to the simplicity of a driver achieved with the specialized integrates.

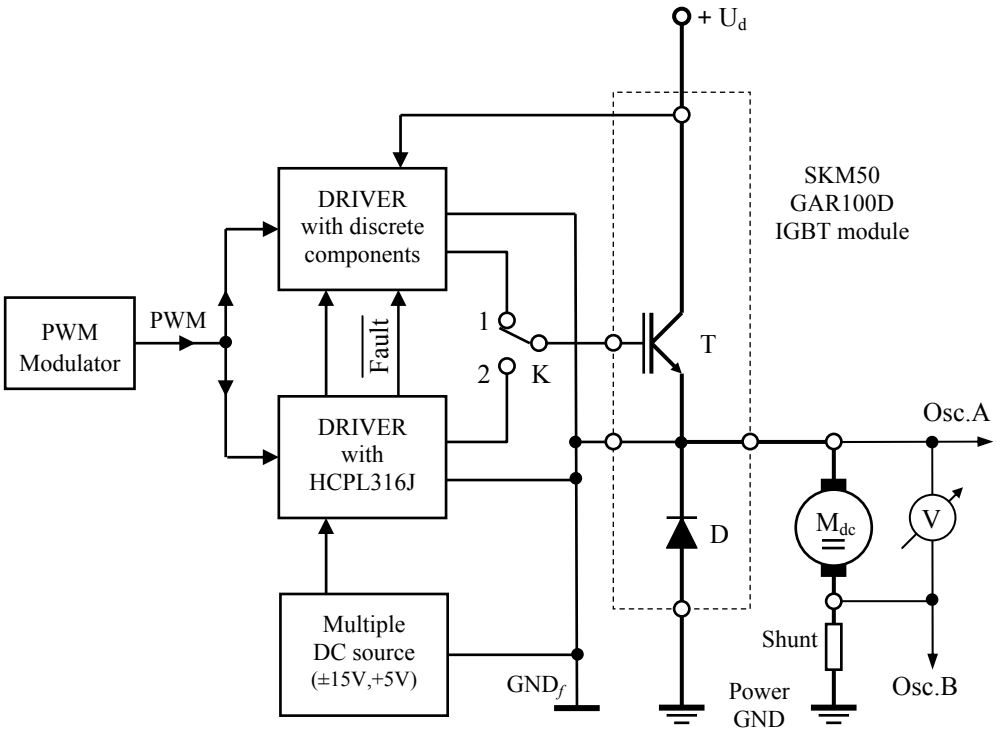

Fig. 5.16 Block diagram of the laboratory application.

The two drivers can control separately the *T* transistor of IGBT type, transistor included in a power module (SKM50GAR100D) together with the *D* recovery diode. The driver selection can be done by means of the K mechanical switch. If K is in 1 position the power MOS gate transistor is controlled by the driver achieved with discrete components and if the K switch is in 2 position the power transistor is controlled by the integrated driver HCPL 316J. The logic control signal applied to the each driver input is generated by a PWM modulator with a logical level of 5V (TTL level). The connection between the modulator and the driver is done with a shielded cable having connectors at each end. Using the *P* potentiometer from the PWM modulator we can modify the duty ratio of the PWM signal.

The integrated driver HCPL316J, among other functions (eg. electrical isolation, undervoltages lookout - *UVLO*) has DESATuration overcurrent protection and fault status feedback. If a fault situation occurs ***the integrated driver stops the PWM control signal and memorizes the fault state***. This feature can be used also by the driver made with discrete components to stop the control signal in the case of a short circuit current occur through the *T* transistor.

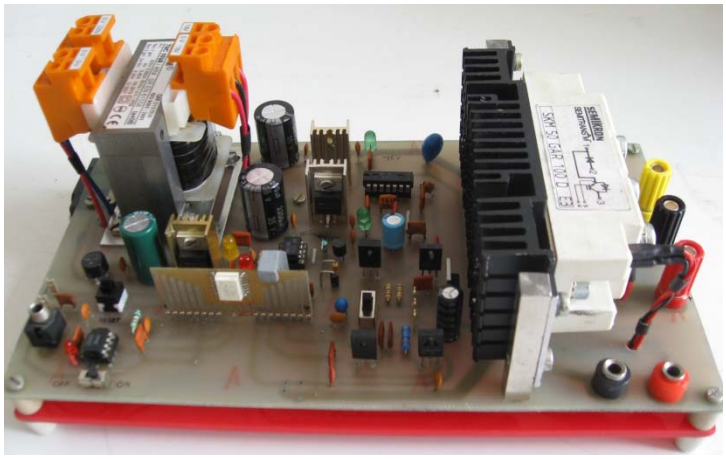

Fig.5.17 Image of the MGD laboratory board.

The internal connection of the power module, between transistor *T* and diode *D,* allows to obtain a one-quadrant chopper which fed the DC motor (M_{dc}) with width modulated voltage pulses. By changing the duty ratio of the PWM signal, it can be modified the average voltage (DC voltage) across the DC motor and thus its speed. This regulated DC voltage can be measured using the voltmeter *V*. The laboratory setup allows to display easily the waveforms of the PWM logic signal, of the gate voltage, of the chopper output voltage and current. In the image of Fig.5.15 the oscilloscope shows the waveforms of the voltage that supply the motor and of the current that flows through it (the shunt voltage).

a) MOS gate driver achieved with discrete components

Fig.5.18 presents a version of a MOS gate driver made with discrete components. Due to economic and performance reasons, it is not recommended to have such implementation as long as it exists on the market a rich and diverse offer of integrated drivers which can be bought at very low prices. However, most of these integrated MGDs do not have all the specific functions of a control circuit, shown previously. Depending on the chosen of the integrated driver and on the application requirements, it may be necessary to complete the entire control circuit with the missing blocks or stages. To achieve this, it must be known as many practical implementation variants of the MGD functions.

The circuit shown in Fig.5.18 implements in a simple way three main functions: electrical isolation, control signal adaptation to the gate's requirements and the overcurrent protection function. In the scheme were not included complex protection circuits and bidirectional communication circuits.

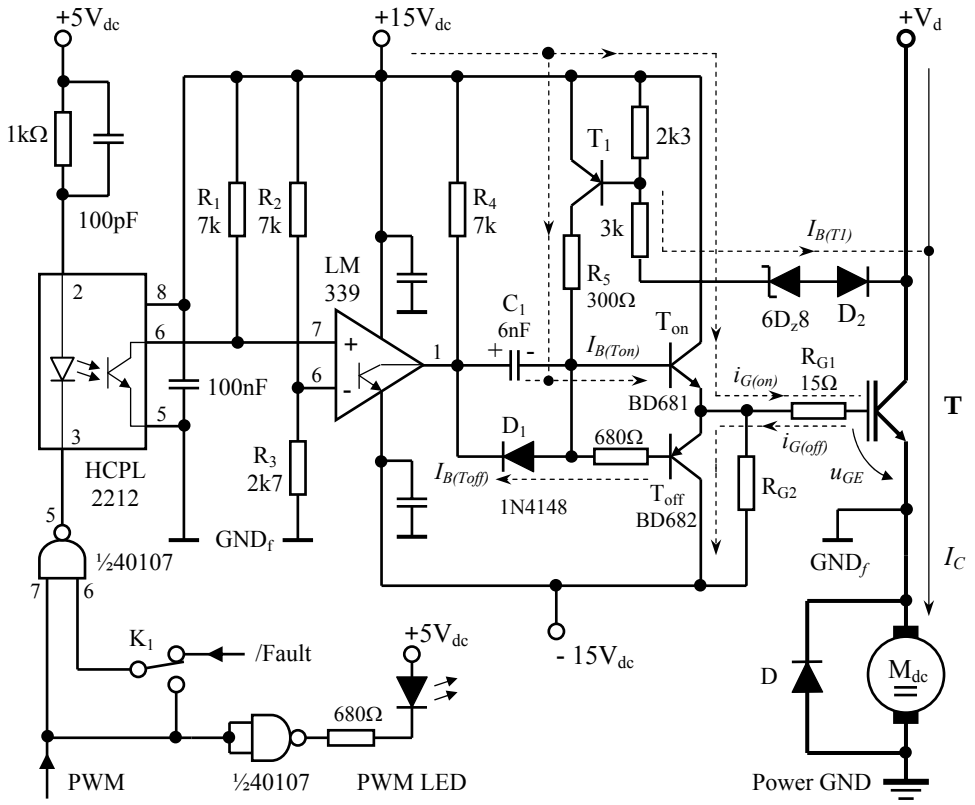

Fig. 5.18 MOS gate driver achieved with discrete components.

The isolation barrier was placed at the entrance of the circuit, on the PWM's signal path. To achieve an electrical isolation, it was chosen the solution of a fast optocoupler HP2212. This is an optocoupler integrated version that includes, besides a photodiode-phototransistor ensemble, other components such as a Triger-Schmitt circuit to restore the transmitted signal shape. The supply voltage for the HP2212 can be in the range of (5 ... 20V) to achieve the desired level of the output signal.

The overcurrent protection uses the technique based on the desaturation phenomenon described above. Fault memory occurs only during the actual switching period. The protection circuit is carried out around the T_1 transistor which maintains the on-state of the T_{on} transistor (BD681) and hence the on-state of the MOS gate power device. At the same time, the on-state of the T_1 transistor depends on the voltage drop $V_{CE(T)}$ across the power transistor (V_{on}). If it leaves the saturation region (ohmic region for MOSFETs) as a consequence of the overcurrent occurrence, the $V_{CE(T)}$ voltage increases and when the following condition is fulfilled:

$$V_{CE(T)} + V_{BE(T1)} + V_{Dz} + V_{D2} \geq V_{G+} = +15\text{V}_{\text{dc}} \tag{5.9}$$

the D_2 diode is reverse biased interrupting the $I_{B(T1)}$ base current of the T_1 transistor. Thus, T_1 and T_{on} are turned off and the power transistor T will enter in a turn-off process, slower than in the case of a normal functioning because the MOS gate is connected to the negative voltage through the two series resistors R_{G1} and R_{G2}.

In order that T_1 transistor can perform the overcurrent protection, first the power device must be brought in on-state. For this purpose, the PWM control signal discrete initiates the conduction of the power transistor. Its on-state is maintained depending on how evolves the load current (I_C), as shown above.

The turn-on initiation of the power MOS gate transistor T is done by activating the optocoupler through the PWM signal. The turn-on information will propagate to the comparator that will turn-off its final "open collector" transistor. Thus, a charging current through the C_1 capacitor appears with the direction shown in the figure. This transient current activates for a short time the T_{on} transistor, that will turn-on the power device T. During the turn-on transition time the voltage drop across the power transistor falls to the saturation value $V_{CE(sat)}$ allowing the Zener diode D_z turn-on and the base current $I_{B(T1)}$ occurrence. By the T_1 transistor turn-on will ensure the base current of T_{on} even after the disappearance of the charging current through the capacitor C_1.

Deliberate turn-off of the power transistor is determined and maintained by the low level (0L) of PWM signal. This off level disables the optocoupler which, in turn, switch the LM339 comparator in the initial state. Thus, the final transistor of the comparator is brought into conduction and at comparator output a negative potential appears given by the negative supply voltage ($-15V_{dc}$). Consequently, the current $I_{B(Toff)}$ appears, first on the path of C_1 capacitor until it is discharged and then on the path of D_1 diode. Therefore, T_{off} transistor (BD682) is turned on and further it turn off the power MOS gate transistor T.

b) MOS gate driver achieved with a specialized integrated circuit

Fig. 5.19 presents the version of a control circuit for a power MOS gate transistor made with the HCPL 316J integrated driver. This is a gate drive optocoupler of Hewlett Packard Company with electrical isolation able to control the power MOS gate transistors (MOSFETs or IGBTs) with *n* channel. TTL logic levels of the inputs allow direct interfacing with complex digital systems (microcontrollers - μC, digital signal processors - DSPs). It performs overcurrent protection functions (desaturation detection V_{CE}), decrease of supply voltages protection (***U**nder**V**oltage **L**ook**O**ut* - UVLO) and fault status feedback. Maximum gate current is $I_{G(max)}$= 2A. It is enough to effectively control any power devices working up to 150A and 1200V. If it is desired to increase the gate current an external amplifier circuit can be used.

Because the logic part of the integrated driver is isolated from the final stage (buffer), there are required two isolated DC voltages for the circuit supply. The *bootstrap* supply technique can't be used because the integrated is not of HVIC type

(***H**igh **V**oltage **I**ntegrated **C**ircuit*). As discussed in section (5) the logic block of the driver is supplied separately with the voltage V_{dc1} = +5V (TTL level), and the final stage is powered by the double DC source with the voltages $U_{G+}=V_{dc2}$=+15V and $U_{G-}=V_E$= -(5÷15)V. It is necessary to take care that the potential difference between the two gate voltages does not exceed 30V.

The electrical isolated barrier is placed inside the integrated driver between logic block and final stage. Benefiting by HP company achievements of the optocouplers, the circuit includes two fast optical paths: first for transmission of the PWM control signal, and the second for the transmission of the fault signal in the case that the protection circuit is activated (from the part connected to the power transistor).

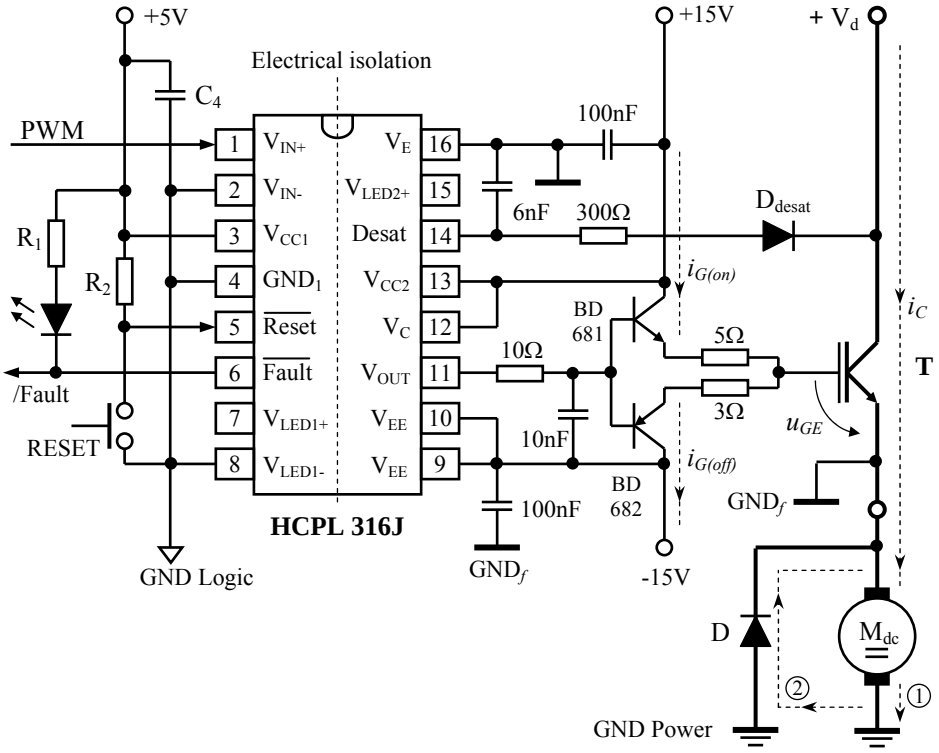

Fig. 5.19 MOS gate driver achieved with the HCPL 316J integrated circuit.

The short circuit protection is of DESAT type. For this, the driver includes a comparator and an internal reference voltage of 7V. As discussed above, it is preferred a gradual power transistor turn-off when an overcurrent appears to prevent switching overvoltages. The HCPL 316J integrated driver uses this solution. Thus, if an overcurrent occurs, a dedicated internal transistor is turned on and it will decrease progressively the gate on voltage of the power transistor. When the threshold of 2V is reached, the internal blocking T_{off} transistor is turned on and it steeply negatives the MOS gate of the power device.

The external circuit used for DESAT protection includes the D_{desat} diode (fast, high voltage) and the R-C filter (300Ω–6nF). The last one allows the rejection of the false fault signals. It introduces a delay in the signal transmission from the collector (drain) to the internal comparator. Thus, the integrated driver receives this feedback signal (on D_{esat} pin) after the power transistor is fully in on-state. The filter resistance also serves to limit the reverse recovery current of the D_{desat} diode and thus to protect the driver.

The overcurrent protection is combined with the supply undervoltage protection (UVLO) in a logical OR condition. Whatever would be the protection that is active, it is transmitted through a feedback optical path for the logic circuit located in the primary side, electrical isolated from the secondary part connected to the power structure. Here, a special circuit memorizes the fault, stops the PWM signal and turns on an internal "open collector" transistor dedicated to communicate outside the fault situation. To obtain the fault logical signal, active on 0L ($\overline{Fault}$), between the corresponding pin and the +5V supply voltage, the R_1 resistance (3,3kΩ) is connected.

It should be noted that the HCPL316J integrated driver is one of the few specialized control circuits that stores on indefinitely the fault and does not reset the fault state at the end of the switching period. Consequently, after notification of a fault, the circuit can be unlocked only from the outside with a logic $\overline{Reset}$ signal, active in 0L, obtained using a button labeled with RESET.

The driver has the possibility of receiving the PWM control signal in an inverted logic, in which will be used the V_{IN-} input. When the PWM signal operates with positive logic, the V_{IN+} input is used, while the V_{IN-} input is connected to the ground, as shown in the figure or can be used an external signal STOP, active in 1L.

Because the IGBT is a relatively high power device, between the HCPL316J output and the transistor MOS gate, it was used as an amplification stage that can support large current pulses for fast charging and discharging the gate capacity. The stage is made with a pair of complementary bipolar transistors BD681/BD682 which can sustain peak collector currents up to 6A. The BD681 *npn* transistor turns on when at the output of the integrated driver V_{OUT} a positive potential appears. Thus, a current pulse arises whose amplitude is limited by the resistance $R_{G(on)}$ (5Ω). The electric charges carried by this current quickly charge the gate capacity of the IGBT's with a positive voltage and turns it on. The on transition time of the IGBT will be shorter when the gate current pulse amplitude will be higher.

The IGBT turn-off is started when the output signal V_{OUT} descends to negative values. Thus, when the *pnp* BD682 transistor is turned on, the MOS gate capacity is quickly discharged and the IGBT is turned off. The role of the $R_{G(off)}$ resistance is to limit the discharge current of the gate capacity. Its value (3Ω) will directly influence the turn-off speed of the IGBT. By maintaining the BD682 transistor in on-state during the entire off time interval of the IGBT, a negative potential is maintained on

the gate terminal, avoiding in this way any accidental transistor turn-on due to disturbances.

The entire laboratory board with the two MOS gate drivers is supplying with a multiple DC source providing at its outputs stabilized voltages of $\pm 15V_{dc}$ and $+5V_{dc}$. These voltages are obtained by rectifying the AC voltages supplied by a line frequency transformer with three secondary windings. After the AC voltages are rectified through the diode bridges, filtered with the help of the electrolytic and ceramic capacitors the DC voltages are obtained which are stabilized using the voltage regulators LM7815, LM 7915 and LM 7805.

7. Objectives and procedures

1. It will be studied the theoretical aspects related to the power MOSFETs and the IGBTs from the first part of the paper: symbols, semiconductor structure, static characteristics, etc.
2. It will be analyzed how through the gate voltage is induced the conduction state (field effect, inversing phenomenon) and which are the standard recommended magnitudes of the gate voltage for the transistors turn-on and turn-off.
3. It will be studied the gate resistors role in the dynamic evolution of the power MOS gate transistors and how their values can be established.
4. It will be analyzed the functional blocks of the MOS gate drivers: final stage, protection circuit, interface and electric isolation circuits, supply sources, etc.
5. It will be analyzed the laboratory board to identify the position of the DC source, of the power module, of the control circuit with the two drivers, of the important discrete components and of the connection terminals.
6. It will be analyzed the driver's operation made with discrete components (see Fig.5.18).
7. It will be analyzed the driver's operation made with the specialized integrated HCPL316J (see Fig.5.19).
8. It will be assembled the laboratory setup whose block diagram and image is presented in Fig.5.16 and in Fig.5.15, respectively. It will be powered and put gradually in to operation, starting with the PWM modulator and the MOS gate drivers.
9. It will be displayed with the help of the oscilloscope, the waveform of the PWM signal and it will be highlighted its level and the possibility to modify the duty ratio with the potentiometer rotation on the PWM modulator.

10. It will be displayed the gate voltage (u_{GE}) waveform given by the two drivers by modifying the *K* switch position. It will be analyzed the levels and the fronts of this signal in comparison with the signal generated by the PWM Modulator. It can be highlighted also the signal propagation delay through the drivers if the two signals are simultaneously displayed using an oscilloscope having two isolated channels.
11. It will be highlighted how the DESAT protection works for each driver by disconnecting the link between the control circuit and the power transistor collector while the gate voltage u_{GE} is displayed.
12. It will be supplied the power structure (the one quadrant chopper) with the V_d voltage and it will be visualized, using an oscilloscope with two spots, the output current (i_o) waveform and the output voltage (v_o) waveform.
13. It will be highlighted the adjustment of the V_o average voltage through the duty ratio of the PWM signal using a voltmeter and also by observing the speed change of the DC motor.

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