Lab no. 6

INTEGRATED MOS GATE DRIVERS

1. Introduction

As presented in the previous laboratory papers (Lab no.5), the power necessary to control the MOS gate transistors is negligible; for this reason, in the modern version, the drivers of these power semiconductor devices (MGDs – **M**OS ***G**ate **D**rivers*) are integrated in complex circuits or in modules with multiple control and protection functions. By using these ***integrated drivers***, the power electronic systems become simpler, more reliable, smaller and lighter.

There is a wide variety of integrated circuits for the MOS gate transistors control (***IC Drivers***), because there are many companies producing these drivers (IR-International Rectifier, IXYS, Semikron, Texas Instruments, HP-Hewlett Pakard etc.) and each of them has a rich offer for different applications.

Next, an approximate classification of the available MGDs will be attempted, so that the interested reader is going to get an overview of the market in this area. The classification will take into account the issues discussed in the previous application and for each category it will be highlighted the examples of the firms' products.

2. Classification of the integrated MGDs

An approximate classification of the IC drivers can be done according to the:

- number of power transistors controlled by the MGD - based on this criterion it can be defined the following types of integrate drivers:
  - IC drivers for a single MOS gate transistor (*Single Channel Drivers*: HCL316J, IR 2117÷IR2128 etc.);
  - IC drivers or MGD modules for two MOS gate transistors (*Half Bridge Drivers* or *High and Low Side Drivers:* IR2101÷IR2113, IXBD4410/4411, SKHI22, 24 modules, 2SD315A, 2ED300C17 etc.);
  - IC drivers or MGD modules for entire bridges (H bridge, three-phase bridge) made with power MOSFETs or IGBTs (*Bridge Drivers*: IR2130, IR2132, SKHI61, SKHI71 etc.).

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- presence or absence of the electrical isolation function – the following integrated drivers can be found:
  - IC drivers or MGD modules with electrical isolation between input and output (*Isolated Drivers*: HCPL316J, SKHI*xx* etc.);
  - IC drivers without electrical isolation constitute a group including the majority of integrated drivers and who their turn may refer to:
    - Low voltage IC drivers (IXBD4410/4411, IXBD4412/4413);
    - ***H**igh **V**oltage **I**ntegrated **C**ircuits* (HVICs) which accept high voltages on some of their terminals (IR 2101÷IR2155);
- number of supply voltages – the following drivers can be found:
  - IC drivers needing isolated supply voltages between the logic side and the final MOS gate stage (HCPL 316J);
  - IC drivers with on-board "negative charge pumps" able to generate their own negative turn-off voltage starting from the positive gate voltage (IXBD4410/4411, IXBD4412/4413 etc.);
  - IC drivers or MGD modules needing a single supply voltage from which, through different techniques (*bootstrap* technique, miniature switching sources) are obtained all the operating voltages (SKHI*xx* modules, IR 2101÷IR2155 etc.)
- number and types of protections functions - there can be defined different categories of integrated MGD as follows:
  - IC drivers which provide a minimum protection such as the overcurrents protection (*DESAT protection*) and/or the voltage supply decreasing protection (UV – ***U**nder**V**oltage protection*), (HCPL316J, IR 2101÷ IR2155 etc.);
  - IC drivers or MGD modules which provide several types of protection, in addition to the minimum requirements, such as: protection to overvoltages (OV- ***O**ver**V**oltage protection*), protection when the negative turn-off voltage disappears (IXBD4410/4411), protection when the dead time disappears (*interlock protection* – SKHI*xx*), protection when the temperature of the power device increases etc.
- capture or not of the fault situation after a protection is activated. According to this criterion may be found the following drivers:
  - IC drivers or MGD modules with automatic RESET that turned off the power transistor, after the fault situation had occurred, only during the actual switching period;

- IC drivers provided with complex logic blocks used for damages treating and memorizing, blocks which will turn-off the power transistor during fault situations, will communicate the fault state to the digital control system and will wait from a release signal (RESET).

- autonomy degree - may be as follows:
  - Actual IC drivers with only limited autonomy to manage the good working conditions within their control area (protection functions). The main role of them is to interface the digital system that generates the logic control signals and the MOS gate of the power transistor;
  - PWM modulators or controllers which operate independently from an external digital control system. These integrated circuits (ICs) contain, besides the proper drivers, a control block capable of generating PWM signals with a fixed or an adjusted duty ratio. In the small powers domain there are numerous ICs that form a special category, different from the MOS gate drivers' category. Depending on the application we can encounter:
    - ICs for the modern electronic ballasts (e.g. *Self-Oscillating Half-Bridge Drivers* IR2151÷IR2166) – 50% PWM duty ratio;
    - ICs for the modern PFC converters – (***P**ower **F**actor **C**orrection Controllers*) – e.g. 38500 series – Texas Instruments (TI);
    - ICs for the switching supplies control – e.g. UC3800 series (TI).

3. Supply possibilities of the integrated MGDs

In the laboratory application no.5, dedicated to the general control aspects of the power MOS gate transistors, it was highlighted an important design criterion that consists in the MGD supply variant. Fig.6.1 shows an example with a control circuit that can operate if it has four different supply voltages: V_{dc1}, V_{dc2}, V_{G+} and V_{G-}. A solution to simplify this problem would be to use the same positive voltage for the logic part supply and also for the final stage ($V_{dc1} = V_{G+}$). Consequently, it is necessary to cancel the isolation function; the amplitude of the supply voltage must as well be optimized for the purpose of the proper functioning of both parts. Not always solutions can be found, because a complex control scheme requires certain standard voltages for the logic circuits and other values for the gate voltages. For example, in order to achieve the $+15V_{dc}$ amplitude on the MOS gate of the power device, the V_{G+} voltage must be higher to compensate the on-state voltage across the T_{on} transistor:

$$V_{G+} = V_{GE(T)} + V_{CE(Ton)} = +(16 \div 18)\text{V} \tag{6.1}$$

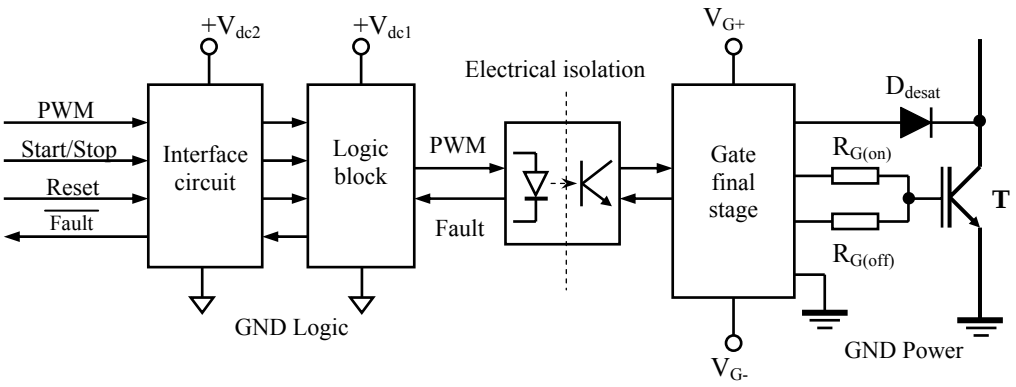

Fig. 6.1 Supply version of a complex MGD.

The negative gate voltage, needed for the MOS gate transistor turn-off, will be chosen depending on the disturbances level in the power electronic system and it can be in the range of:

$$V_{G-} = -(5 \div 15)V_{dc} \tag{6.2}$$

If the electrical isolation is done before the final stage, the gate voltages (V_{G+}, V_{G-}) must be isolated from the other voltages which supply the logic and the interface blocks – Fig.6.1. Also, in the MGDs logic side may be needed more supply voltages. It is possible that some blocks which included the IC driver, to require a supply voltage of 15V (V_{dc1}) and the interface circuit with the external digital control system to operate with logic signals of TTL level (V_{dc2} = 5V).

From the foregoing, it can be said that in order to solve the supply problem of a single control circuit, there are needed two isolated DC sources, of which at least one must be able to provide more voltages. The problem becomes more complicated if the power structure contains more power transistors. For some of these transistors, the control terminal is reported to a floating ground. This is the case of the high (upper) device from the half bridges structure, T_1 transistor in Fig.6.2.

The two transistors from the half bridge topology are mandatory controlled in contretemps. During the T_1 on-time interval, the T_2 is off and vice-versa. When T_2 is on, the potential of the floating ground GND_f is closed to the GND *Power* potential and when T_1 is on the GND_f potential increases to the $+V_d$ value. Due to the potential variation of the GND_f each IC driver (*High Side Driver* and *Low Side Driver*) must have its own DC source. In turn, each source must be double, in order to supply the pair of voltages ($U_{G+(1)}$, $U_{G-(1)}$) and ($U_{G+(2)}$, $U_{G-(2)}$), respectively.

The sides of all IC drivers, electrically isolated from the power structure, can be cumulated into the same logic circuit, supplied by the same DC source, as shown in the block diagram of Fig.6.2. In conclusion, to control a half bridge in a usual way,

without IC drivers presenting supply facilities, there are required three isolated sources, out of which at least two must be double.

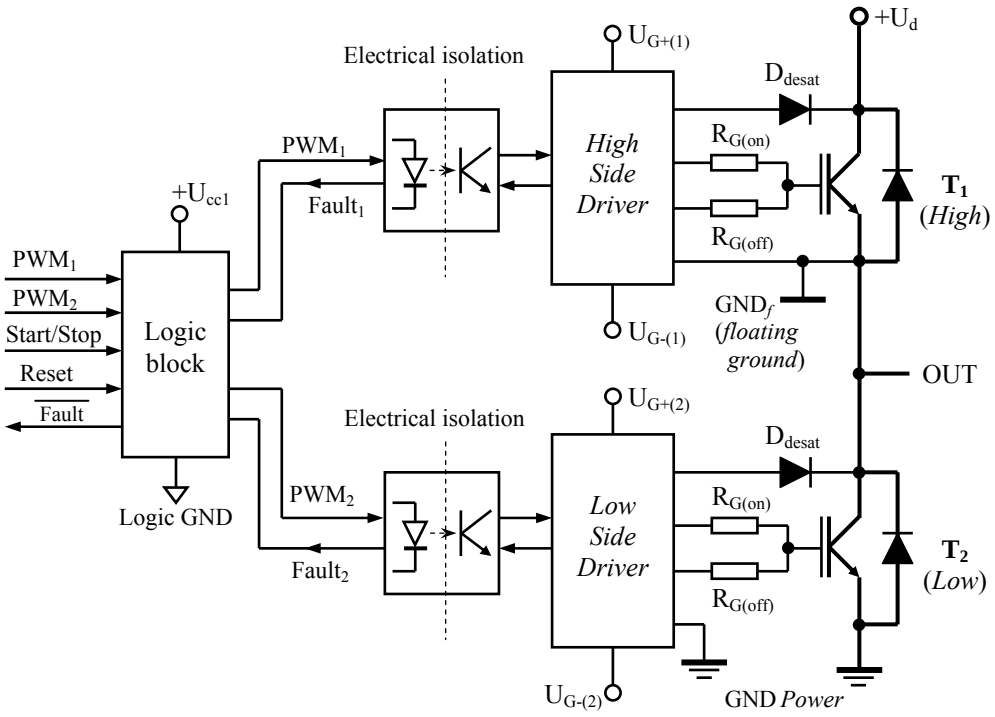

Fig. 6.2 Supply version of the drivers for a half bridge structure with MOS gate transistors

The number of DC sources raises to five if a three-phase bridge is controlled. The three-phase bridge contains three legs (half bridge structures). Every driver for the high transistors required a double DC source. An economy is obtained for the low (bottom) transistors, because all the drivers are reported to the same ground (GND *Power*), so only a source is needed. If the source from the isolated side of the driver (logic block) is considered, five DC sources are obtained. A positive aspect of such a high number of sources is their low power.

To solve the supply problem for the MOS gate drivers from a complex power electronic system, two options are available to the designer:

- Using a regulated multiple DC source with an adequate number of outputs, electrically isolated. The source can be linear with a line-frequency transformer having more isolated secondary windings. It is a classical solution suffering in terms of size, weight and efficiency. The modern alternative is to use a switch-mode power supply with isolated multiple outputs, source that eliminates the disadvantages of the linear sources;

- Using integrated MGDs specially designed to reduce the number of the sources and the supply voltages.

In turn, the integrated MGDs are available on the market with different supply facilities:

- MGD modules which contain in their structure DC switching supplies (microsources) with isolated outputs, which, starting from an unique DC voltage, generate all the necessary voltages;
- IC drivers with *"negative charge pumps"* with which, from the positive gate voltage (U_{G+}), generate the turn-off negative voltage U_{G-};
- IC drivers able to operate at floating potentials from which can be obtained the positive gate voltage (U_{G+}) with the help of bootstrap technique from the voltage that supplies the logic block.

The MGDs with isolated DC microsources are achieved with high frequency transformers that cannot be included in integrated circuits. For this reason, we find these MGDs on the market in the form of modules, in open case or encapsulated (see SKHI*xx* modules).

The IC drivers provided with negative charge pumps contain a simple switching structure, capable to accumulate charges on the armatures of a "reservoir" capacity, on which it is obtained the negative turn-off voltage.

There are some IC drivers which operate at floating potentials and which can be supplied with a single voltage. This performance is obtained using the so-called ***bootstrap technique***. Fig.6.3 shows an implementation of this technique for an IC driver (IC_1) that controls the high transistor from the half bridge structure. The IC_1 driver is not of HVIC type and requires isolated circuit elements on the informational path in order to avoid the high voltages.

The supply *bootstrap* technique is based on a very small consumption of the IC drivers. Thus, in a short time interval, according to the switching period (tens ÷ hundreds of μsec), the power fed can be provided by a small reservoir such as the C_b capacitor. Each time when the low transistor (T_2) of the half bridge structure is on, the GND_f floating ground of the high integrated circuit IC_1 is connected to the power GND. Therefore, the I_{Cb} current flows on the path shown in Fig.6.3. This current charges the C_b capacitor and the U_{G+} supply voltage occurs. By choosing a minimum value for the limiting resistance R_b, it is obtained a small time constant of the R_1–C_1 circuit, so that, for a very short on-time interval, the T_1 transistor manages to charge the C_b capacitor. In the next time interval, the T_1 power transistor is off and the T_2 is on. During this time interval the driver IC_1 is supplied by the C_b. After a switching

time period, T_2 is turned off, T_1 is turned on again and the C_b capacitor can recover the power lost in the previous time interval.

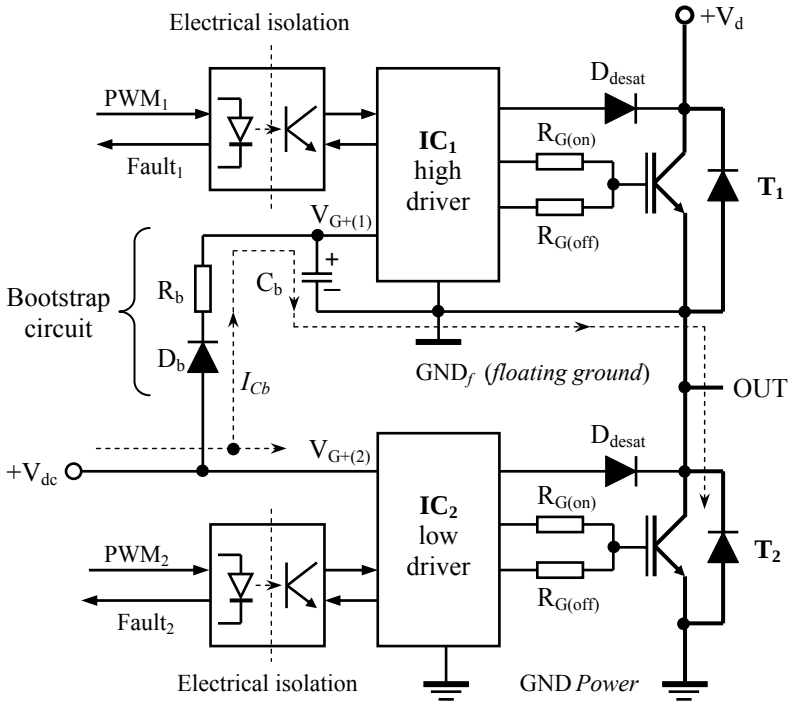

Fig. 6.3 Bootstrap technique to supply the IC driver (IC_1) for the high transistor of a half bridge structure.

The D_b diode has the role to protect the U_{G+} source and the lower driver IC_2 against the high voltage V_d when the power transistor T_1 is in on-state. There should be a fast switching diode with high V_{RRM} (maximum reverse repetitive voltage).

If it is desired that the power MOS gate transistor to be turned off with a negative voltage it will be used an IC driver with the "negative charge pump" for the V_{G-} voltage generation.

The supply *bootstrap* technique is also used by the IC drivers of HVIC type which do not require circuit elements for electrical isolation on the informational path. In Fig 6.4 is shown the supply method of such double driver (*high and low driver*) dedicated to control both transistors of the half bridge structure. It has been chosen the cheaper option for which all the necessary voltages of the circuit are given by a unique DC source. For a more secure version, in order to avoid possible control errors, a separate source can be chosen for the logic block.

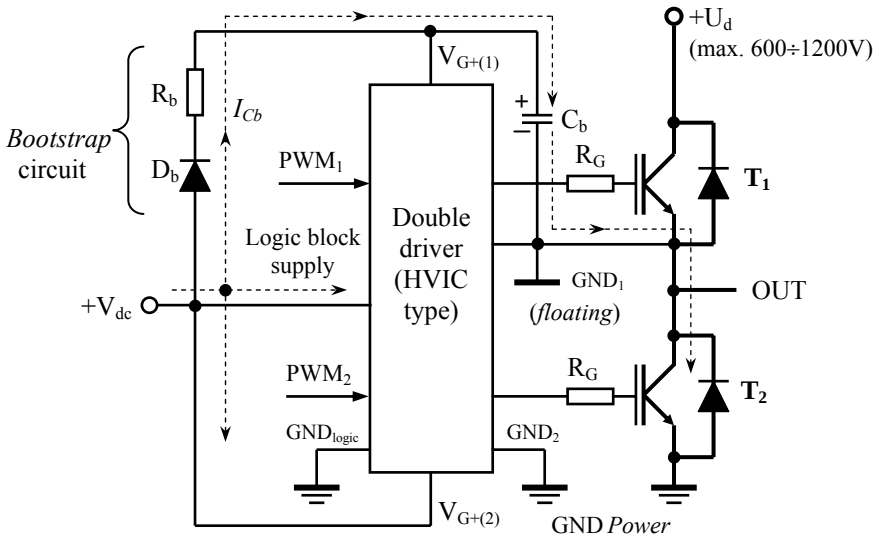

Fig. 6.4 Bootstrap technique to supply a double driver of HVIC type that controls a half bridge structure achieved with power MOS gate transistors.

4. Control technique of a half bridge structure

Generally, in power electronics a half bridge (leg) structure is made up of two power semiconductor devices connected in series. The two devices can be diodes, thyristors, or controllable devices (transistors). When the half bridge is achieved with power transistors and the structure is used for voltage-source converters, the two transistors T_1, T_2 must be provided with antiparallel recovery diodes D_1, D_2, as shown in Fig. 6.2, 6.3 and 6.4. Usually, the output of the leg is the median point of the topology (the transistors connection point). It must be mentioned that, the version of the half bridge with the power transistors is widely used in the switch-mode converters. This version has the great quality to impose the output voltage value only through the on-state combination of the two transistors, no matter the output current's direction flow.

The control of the T_1, T_2 transistors from the half bridge topology must be done in contretemps to avoid the simultaneous conduction of the two transistors, otherwise a short circuit through the transistors of the V_d power supply can appear. Thus, when a transistor is turned on, the other must be in steady off-state and vice versa. If the control of the transistors is periodically with the help of two *width modulated signals*, PWM_1 for T_1 and PWM_2 for T_2, the two control signals appear as shown in Fig 6.5 and are named ***complementary*** (***nonoverlapping***) **PWM *signals***. The time period $T_s=1/f_s$ is called switching period, and f_s is the ***switching frequency***. In applications f_s = (kHz ÷ hundreds kHz) depending on the type of the controllable devices from the half bridge structure.

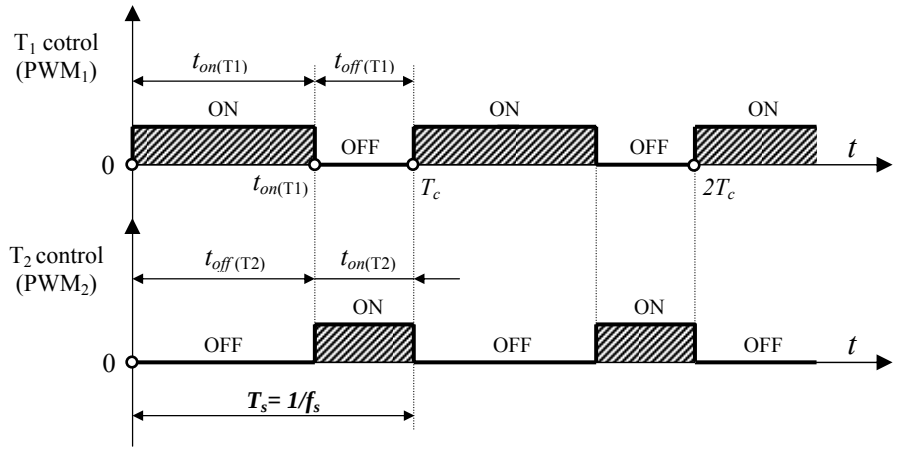

Fig. 6.5 The complementary PWM control signals for the transistors of a half bridge (ideally transistors are considered → they switch instantaneously).

In fact, the power transistors do not switch instantaneously and usually the turn-off transition time is greater than the turn-on transition time. To avoid an overlap conduction of the both transistors (a crossover situation), in practice the two complementary PWM signals from Fig. 6.5 are changed as shown in Fig. 6.6. First is turned off the transistor who was in on-state, next it is expected a ***dead time*** (***blanking time- t_b***) so that it turns firmly off, then the other transistor is turned on. Thus, the signals become *complementary with dead time*. The dead time value is based on the transistors switching speed. In the case of the fast transistors as the MOSFETs, the dead time can be (1÷2)μsec and for the usual IGBTs can be (2÷4)μsec.

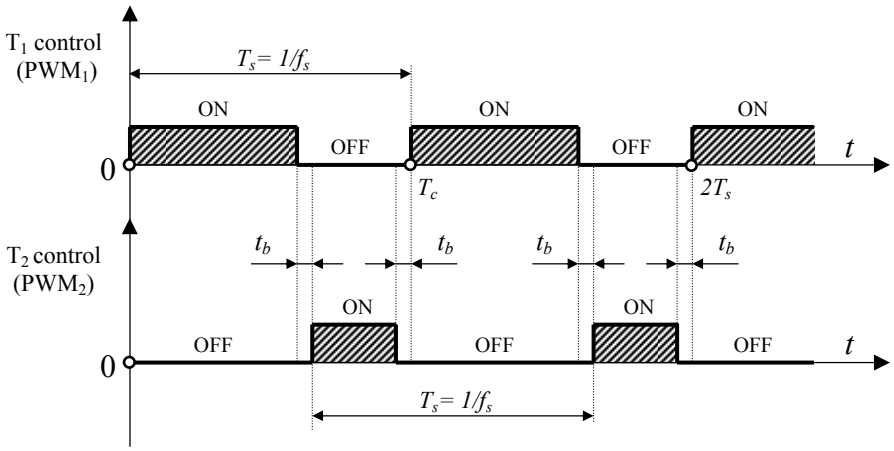

Fig. 6.6 The complementary PWM signals with dead time (blanking time) for a "half bridge" control in real applications.

Since the presence of dead time complicates the analysis of the power structures and the calculation of output voltage values, in the specialized treaties the basic structures of converters are analyzed under ideal conditions, considering that the power transistors switch instantaneously and the control signals can be complementary, without dead time, as shown in Fig. 6.5. Under these conditions, it is obtained the following relation between the duty ratios (D) of the two transistors:

$$t_{on(T1)} + t_{on(T2)}) = T_s \quad \Leftrightarrow \quad \frac{t_{on(T1)}}{T_s} + \frac{t_{on(T2)}}{T_s} = 1 \quad \Rightarrow$$

$$D_{(T1)} + D_{(T2)} = 1 \tag{6.3}$$

The analysis of dead time influence on the power structures operating can be done in separate sections. Also, in these sections are revised the equations obtained under ideal conditions to see how they change in the presence of dead time.

5. MOS gate driver modules

In the Power Electronics Laboratory there are available several MOS gate drivers (MGDs) made with the help of specialized integrate circuits or modules. For this laboratory application is used a control circuit for two transistors, achieved with a MGD module (SKHI22) manufactured by *Semikron Company*. The SKHI family modules were designed to control more medium power MOS gate transistors (IGBTs): 2 transistors (SKHI 22, SKHI 23), 6 transistors (SKHI 61), 7 transistors (SKHI 71) [*www.semikron.com/skcompub/en/drivers-153.htm*]. These modules are some of the most complex, completed and successful control circuits of this type available on the market. They have all the specific qualities of the modern drivers: transmission with electric isolation in the forward direction of the control PWM signals and in reverse direction of the fault signals, entire module supply with a single voltage, power transistors turn-off with negative voltage, rejection of the short control signals, DESAT short-circuit protection, soft short-circuit turn-off, "dead time" missing protection (*interlock* protection) and supply voltage monitoring (*undervoltage lockout* - UVLO - protection).

SKHI 22 hybrid drivers family

The SKHI22 series are hybrid MGDs (modules) made in several variants: SKHI22A, SKHI22B, SKHI22A/B H4. They can control two medium power MOS gate transistors (*double driver*) connected at different potentials. The module notion is used, because this complex MGD is an ensemble placed in a capsule where are working together integrated circuits, pulse transformers or optocouplers, electrical isolated micro-sources and other circuit elements, as shown in Fig.6.7. Because of this compact and hybrid construction (*hybrid dual IGBT driver*), it is obtained several high-performance MGDs, very easy to use in practice.

The modules that include in their code the **A** letter accept on the inputs P12 and P8 (CMOS compatible) PWM control signals with the magnitude of 15V (equal with the supply voltage V_s) and the modules labeled with the **B** letter are controlled with 5V magnitude PWM signals. Also, if in their code is included the **H4** combination, it is a clue that the module can control the power transistors supplied with voltages up to 1700V. Those without this letter combination can work up to voltages of 1200V.

Fig. 6.7 shows the functional block diagram of the SKHI22 dual driver and how this module is connected to the power half-bridge structure made with the IGBT transistors (T_1, T_2).

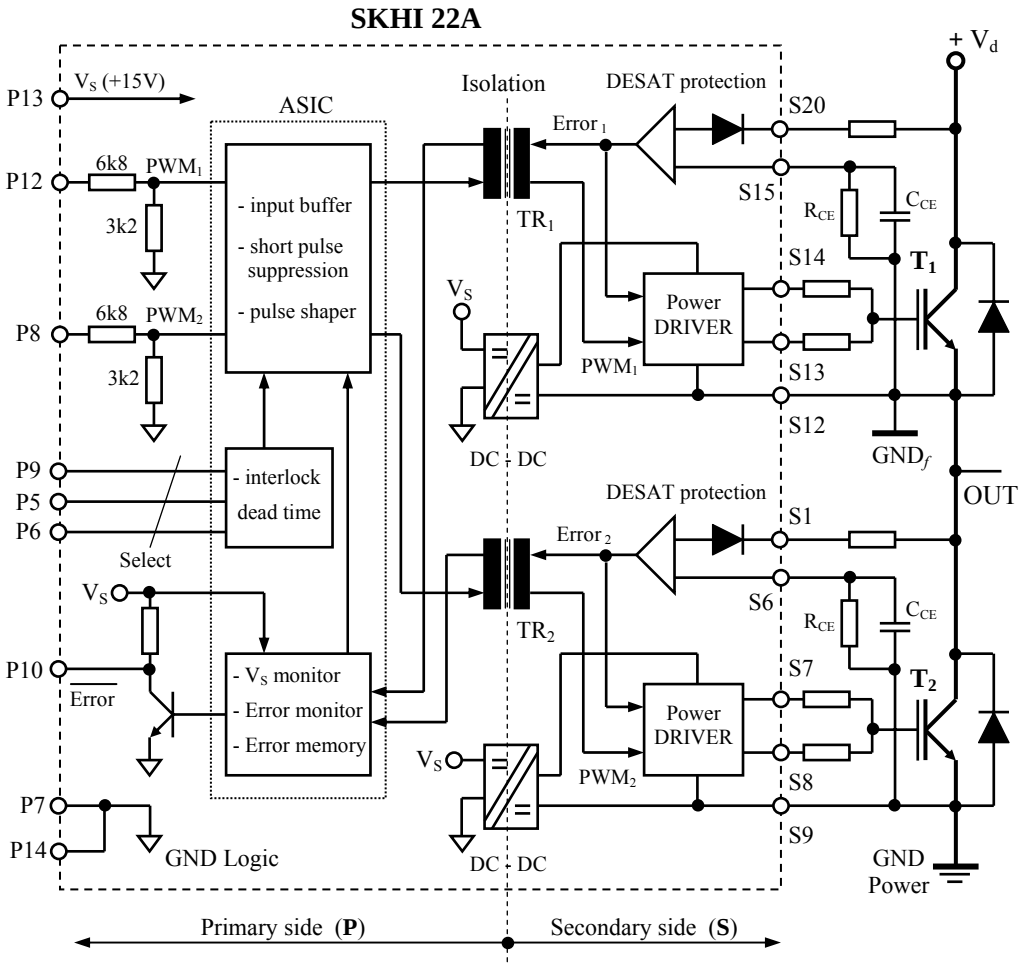

Fig. 6.7 The functional block diagram of the hybrid dual driver SKHI 22A/B (*Semikron* catalogue: *www.semikron.com/products/*).

According to the block diagram the module can be divided into two sides:

- ***Primary side*** (P) that includes the interface block (input buffer, short pulse suppression and pulse shaper), the control block (interlock dead time setting) and the logic protection block (V_s monitor, error monitor and error memory). The DC/DC switching supplies and the pulse transformers (TR_1, TR_2) are the ones which make the isolated connection between the two sides.

- ***Secondary side*** (S), which, in turn, can be splitted into two isolated and identical parts. Each of this part is dedicated to control and protect a power transistor. So, we recognize in these parts the final gate stage (power driver) and the short-circuit protection block (DESAT protection).

A great advantage of these modules is to use a single supply voltage V_s =15V. This voltage supplies the primary side and the secondary side through the two isolated DC/DC micro-sources.

The interface receives the complementary PWM signals with dead time (PWM_1, PWM_2), amplify *(input buffer)* and reshapes them *(pulse shaper)*. Also, the block suppresses the on signals shorter than 500nsec *(short pulse suppression)*. It is a useful function, because the power transistors are not fast enough to react at very short control signals.

The *interlock dead time* block is very useful when, due to the perturbations or due to an incorrect control in the waveforms of the control signals PWM_1 and PWM_2, overlaps occur during the high logic level. This is equivalent with the simultaneous turning on of both transistors and a short circuit through them. To avoid this situation, it was provided this dedicated block that inserts the dead time if it is missing. Its value can be selected between (1,3÷4,3)μsec through a logic combination applied to the three terminals P5-P6-P9.

The monitoring and error memory block (*V_s monitor, error monitor, error memory*) allows the centralization of the received fault messages from the DESAT protection blocks and from the undervoltage protection (*V_s monitor*), storing the fault states, blocking the control signals and communicates to the exterior the fault situation through the $\overline{Error}$ signal. Undervoltage protection works only if the V_s supply voltage decreases below 13V.

All the blocks from the primary side which processes the logic signals are included in a large integrated circuit of ASIC type (***A**pplication **S**pecific **I**ntegrated **C**ircuit*) with the help of which the capsule size are substantially reduced.

The protection against short circuit currents is of DESAT type. The reference voltage V_{ref} applied to the inverting input of the internal comparator can be fixed through the exterior resistance R_{CE} based on the manufacturer equation:

$$U_{ref}[\mathrm{V}] = (9 \cdot R_{CE}[\mathrm{k\Omega}] - 25)/(10 + R_{CE}[\mathrm{k\Omega}]) \qquad (6.4)$$

Choosing R_{CE} =20kΩ it results V_{ref} = 5V.

The minimum time t_{min} left between the moment when the power transistor is turned on and the moment in which the DESAT protection circuit is activated can be adjusted by the capacitor value C_{CE}. The same time value is used for rejecting the false signals from the v_{CE} voltage waveforms. The value of the capacitor C_{CE} can be calculated with the equation:

$$t_{\min} = \tau_{CE} \cdot \ln\left\{(15 - V_{ref})/(10 - V_{ref})\right\} \tag{6.5}$$

where: $\tau_{CE}[\mu\text{sec}] = C_{CE}[\text{nF}] \cdot 10 \cdot R_{CE}[\text{k}\Omega]/(10 + R_{CE}[\text{k}\Omega])$.

For t_{min} = 6μsec, V_{ref} = 5V and R_{CE}=20kΩ it results $C_{CE} \cong$ 1nF.

The configuration of the final stage allows the control with two gate resistors through which can separately be adjusted the turn-on and turn-off transitory times of the power MOS gate transistor.

6. Laboratory application

To emphasize some practice aspects related to the use of the IC drivers or MGD modules in complex topologies made with elementary „half bridge" structures, it will be performed a laboratory setup as shown in Fig.6.8 (image Fig.6.12). The main block of the experimental application is the control circuit obtained with the help of two integrated MGD modules SKHI22H4 and SKHI23, respectively. These drivers are similar in terms of operation (only the type of assembly differs). Each of these modules can simultaneously control two power MOS gate transistors connected into a half bridge structure. Thus, with the help of the entire laboratory control circuit it can be controlled four power transistors or two legs forming a full bridge structure. In the present application the control circuit will be only half used, respectively it controls only one half bridge structure made with IGBT transistors. These power semiconductor devices are integrated in a power module, which is mounted on a radiator that, in turn, sustains the connecting terminals. If we supply the half bridge as in Fig.6.8 we will obtain a four-quadrant DC/DC converter (chopper). The analysis of the static converter operation is not subject of this application and it is presented in the Lab no.18 dedicated to the four-quadrant choppers – half bridge structure.

It is noted that, for the half bridge supply is used a double DC source with two equal voltages: $V_{d1} = V_{d2} = 30\text{V}_{\text{dc}}$. The chopper load is a DC motor that is connected between the output of the half bridge structure and the power GND. The electrical machine is a permanent magnet (PM) DC motor. The rating voltage is 30V_{dc}.

Because the DC/DC converter shown in Fig.6.8 operates in four quadrants, the average value of the output voltage V_o can be reversible and the average output current I_o can be bidirectional. It follows that the converter load (the DC motor) will operate in all four quadrants of the mechanical plan: electromagnetic torque – rotation speed

(T_e - n), which is equivalent with the possibility of rotating and braking (electrical) the motor in both directions.

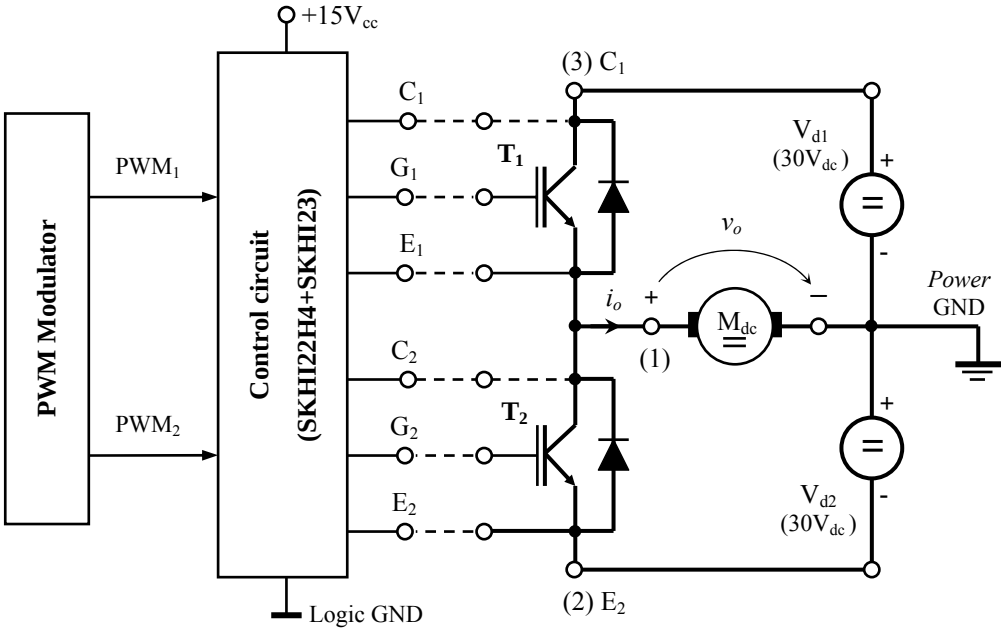

Fig. 6.8 Laboratory setup for study a hybrid dual MOS gate driver (MGD module) (four-quadrant chopper – half bridge structure).

The adjustment of the average output voltage (DC voltage) can be done through the duty ratio of the two power transistors from the half bridge structure. Thus, for:

$$0 \le d_{(T1)} < 0{,}5 \quad \Rightarrow \quad -V_d \le V_o < 0$$

$$d_{(T1)} = d_{(T2)} = 0{,}5 \quad \Rightarrow \quad V_o = 0$$

$$0{,}5 < d_{(T1)} \le 1 \quad \Rightarrow \quad 0 > V_o \ge +V_d$$

The two complementary PWM signals with dead time are generated by a PWM modulator that is connected to the control circuit via a cable provided with standard 9 pins couples at the ends. The waveforms of the PWM control signals and output voltage $v_o(t)$ are shown in Fig.6.9.

Control circuit achieved with the SKHI modules

As has been shown above, the laboratory control circuit includes two MGD integrated modules, one in open construction (SKHI 23) and the other in a closed construction (SKHI 22H4). They were placed from didactics reasons, for comparison, on the same circuit board.

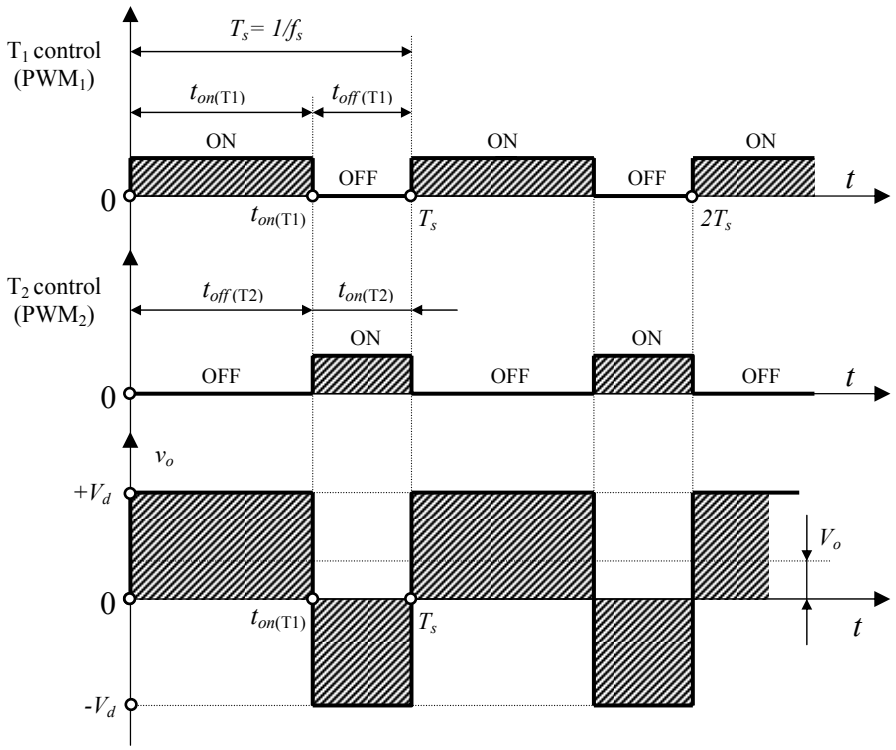

Fig 6.9 Waveform of the output voltage $v_o(t)$ generated by a four quadrant DC/DC converter (half bridge structure) controlled with the help of the studied integrated driver.

By observing the open construction driver, it can be identified a certain circuit elements, it can be appreciated the complexity of these modules and the high-tech manufacturing. Each module can simultaneously control two power transistors included in a half-bridge structure. The PWM control signals applied on the input of the SKHI module can be taken from any type of modulator through the shielded cable or a ribbon cable. To receive PWM signals from great distances, the manufacturer provided the SKHI modules with control inputs of a 15V level in order to reduce the influence of the disturbances. Because the PWM logic signals are generated by the modulators or by the digital control systems (μCs, DSPs) having the level of 5V (recently 3,3V), it was used an adaptation circuit to perform the translation from this logic level to the level of 15V accepted by the modules. The outputs of the control circuits compatible with the MOS gate of the power transistors (+15V for the turn-on, -8V for the turn-off by the SKHI23, respectively -15V by the SKHI22H4) can be taken trough wires with banana plug connectors.

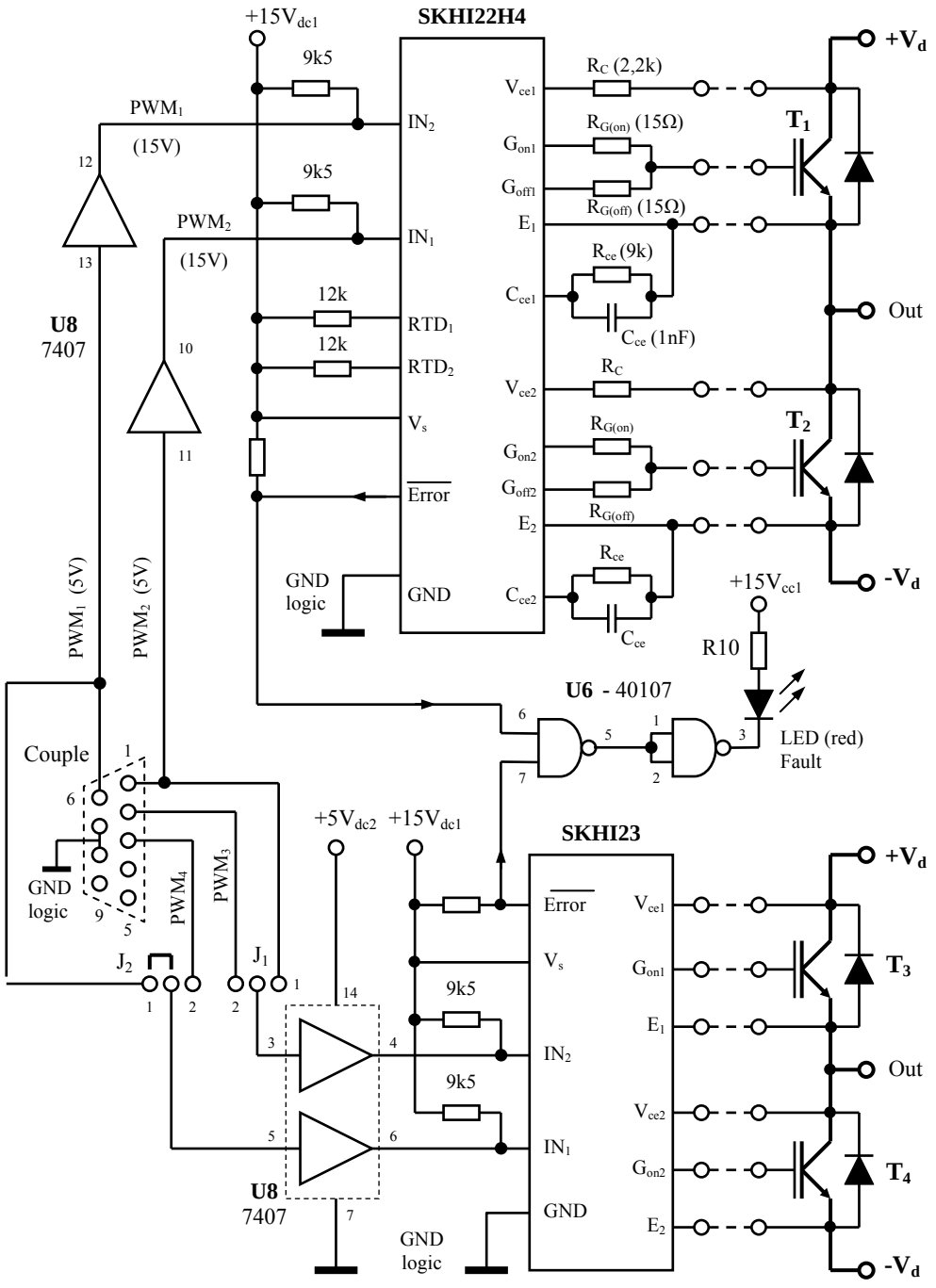

Fig. 6.10 MOS gate control circuit achieved with the SKHI 22 H4 and SKHI 23 modules.

Fig 6.10 and Fig. 6.11 show the block diagram, respectively the image of the control circuit achieved in laboratory with SKHI modules. The module SKHI22H4 being encapsulated, requires an external scheme by which the user can choose, in the secondary side, the gate resistances ($R_{g(on)}$ for turn-on and $R_{g(off)}$ for turn-off) and the delay time after which the short circuit protection (DESAT) becomes active through the R_{ce}-C_{ce} group. In the primary side of the module, through the R_{TD} resistances can be set to the minimum dead time value of the two complementary PWM signals, PWM_1 and PWM_2. In the case of the SKHI23 module achieved on an open printed circuit board, the circuit elements mentioned above can be modified directly, because the manufacturer has provided this facility.

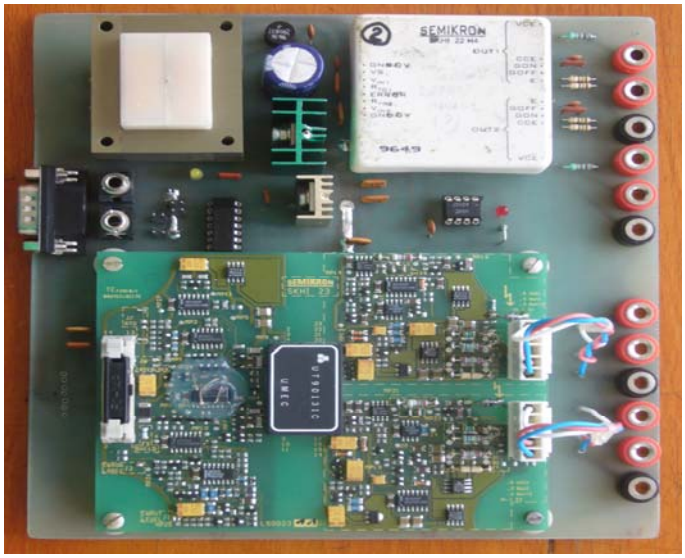

Fig 6.11 The image of the control circuit achieved with SKHI hybrid dual drivers.

The adaptation circuit of the PWM signals level from the 5V to 15V is implemented with the help of the 7407 integrated hex buffers with open collector outputs. The two SKHI modules can be controlled simultaneously with two signals PWM_1 and PWM_2 or controlled separated with the $PWM_1 \div PWM_4$ signals. The variant selection can be done with the help of two jumpers (J1, J2), as shown in Fig.6.10.

The SKHI control modules present multiple protection functions. If one of these is activated, the integrated MGD warns the hierarchically superior control system that a fault occur by sending an error signal (/Error) zero logic 0L active (output of open collector type). In the case of the laboratory control circuit, the error signals provided by the two modules are summed by the NAND logic circuit (40107) which further activates another logic circuit of the same type and light a LED to inform that a fault situation occurs. In this way, can be tested the protection functions of the integrated MGD modules.

To supply the two MGD modules with a single voltage of 15V, it is used a regulated DC source that includes a line-frequency transformer, a single-phase bridge rectifier, a capacitive filter and a voltage regulator LM7815. From the 15V voltage through another voltage regulator LM7805, is obtained the 5V voltage to supply the 7407 hex buffer.

7. Objectives and procedures

1. It will be reviewed from the previous laboratory paper (lab no.5) the theoretical aspects referring to the MOS gate transistors control, the control circuits' operation and their functional blocks.
2. It will be identified the variants of the IC drivers and the MGD modules on the market analyzing the classification of these integrated MOS gate drivers;
3. It will be reviewed the supply options of the integrated MOS gate drivers depending on the controlled power structures;
4. It will be analyzed the control technique of a half bridge topology with complementary PWM signals under ideal conditions and with dead time (blanking time) complementary PWM signals in practice (real conditions).
5. It will be analyzed the block diagram of the MGD module SKHI22 made by Semikron and it will be identified the additional circuits which accompanies this hybrid dual driver ;
6. It will be analyzed the block diagram of the laboratory setup presented in Fig.6.8 and the control circuit board achieved with the two SKHI modules presented in Fig.6.10 (the image in Fig.6.11);
7. It will be performed the laboratory setup which block diagram is shown in in Fig.6.8.
8. It will be displayed, with the help of a two spots oscilloscope, the waveforms of the two complementary PWM signals with dead time generated by the PWM modulator (see the measure points on the modulator printed board);
9. In the conditions in which it will be powered only the control circuit, it will be displayed the waveforms of the gate control voltages (u_{GE}) corresponding to the two transistors from the bridge structure;
10. It will be highlighted how the DESAT protection works by displaying a gate voltage waveform and interrupting the connection between the driver and the IGBT collector (the red LED is lighted);
11. It will be noticed the fault memory during only the actual switching period (the PWM signals blocking until the end of the switching period) and the reset of the fault state after zero crossing of the two PWM signals during the dead time;

12. It will be supplied the power structure (the IGBT half bridge) with the $V_{d1}=V_{d2}$ voltages and it will be displayed with the help of the oscilloscope the waveform of the u_o voltage from the half bridge output which must be like in Fig.6.9.

13. It will be highlighted the variation of the DC voltage V_o (average value) from the converter output with the help of a voltmeter and by notification of the DC motor speed changing in both directions. To modify the V_o voltage it must be adjusted the duty ratio of the two power transistor (width modification of the PWM control signals).

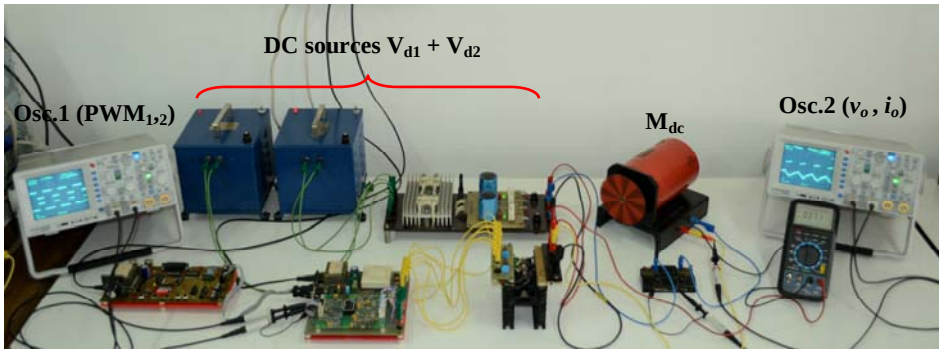

Fig. 6.12 Image of the laboratory application.

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